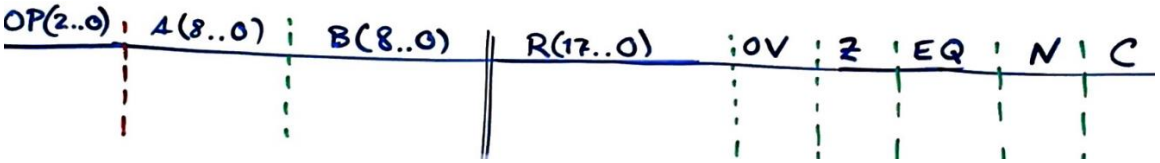
UPC. EETAC. Bachelor's degree. 2A. Digital Circuits and Systems (CSD). **Exam 1.** Grades available by 7th November.
Questions about exams and corrections: office time. **31st October**

(Problem 1) and (Problem 2) and [(Problem 3) or (Problem 4) or (Problem 5) or (Problem 6)]

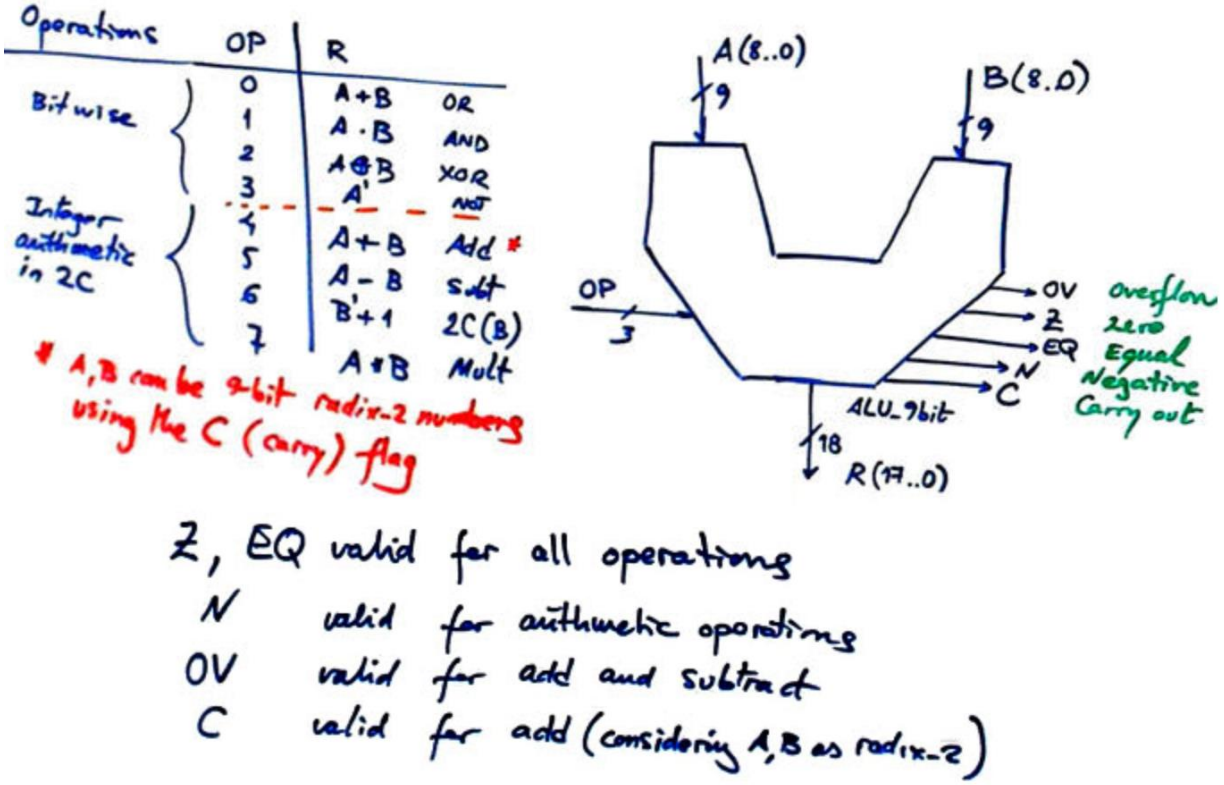
Problem 1 (4p)

The *ALU_9bit* shown in Fig. 1a was used in our LAB4_2 as an example of prototyping and final implementation configuring a target FPGA and designing printed circuit boards (PCB).

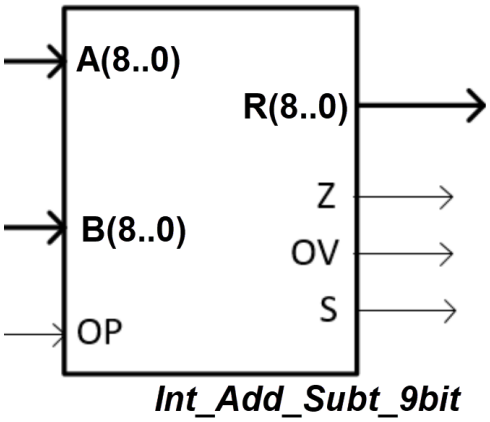
1. Complete the eight operations in binary for the following operands indicating as well the flag values (check your results in decimal when possible): **A** = "011111111"; **B** = "100000001"



2. The circuit, designed internally using plan C2 contains several chips and logic circuits; one of them is the chip *Int_Add_Subt_9bit*, as shown in Fig. 1b, to perform additions and subtractions of 9-bit integer numbers in 2C. Draw a sketch plan for this component. How many VHDL files will include this component?
3. Another component that we can find is the *Adder_1bit*. Design it using plan C2 and the MoD.
4. Design again the *Adder_1bit* using plan C2 and the MoM including a *MUX_8* and a *MUX_2*.



a)



b)

Fig. 1. a) 9-bit arithmetic and logic unit; b) one of its internal chips used for performing arithmetic operations.

Problem 2 (2p)

1. Analyse the circuit in Fig. 1 using method I to obtain its truth table Z = *f*(D1, D0, A, B). Firstly, explain your plan and the concepts and procedures involved in the deduction.
2. What is the circuit's power consumption running at the maximum speed if implemented using CMOS gates?

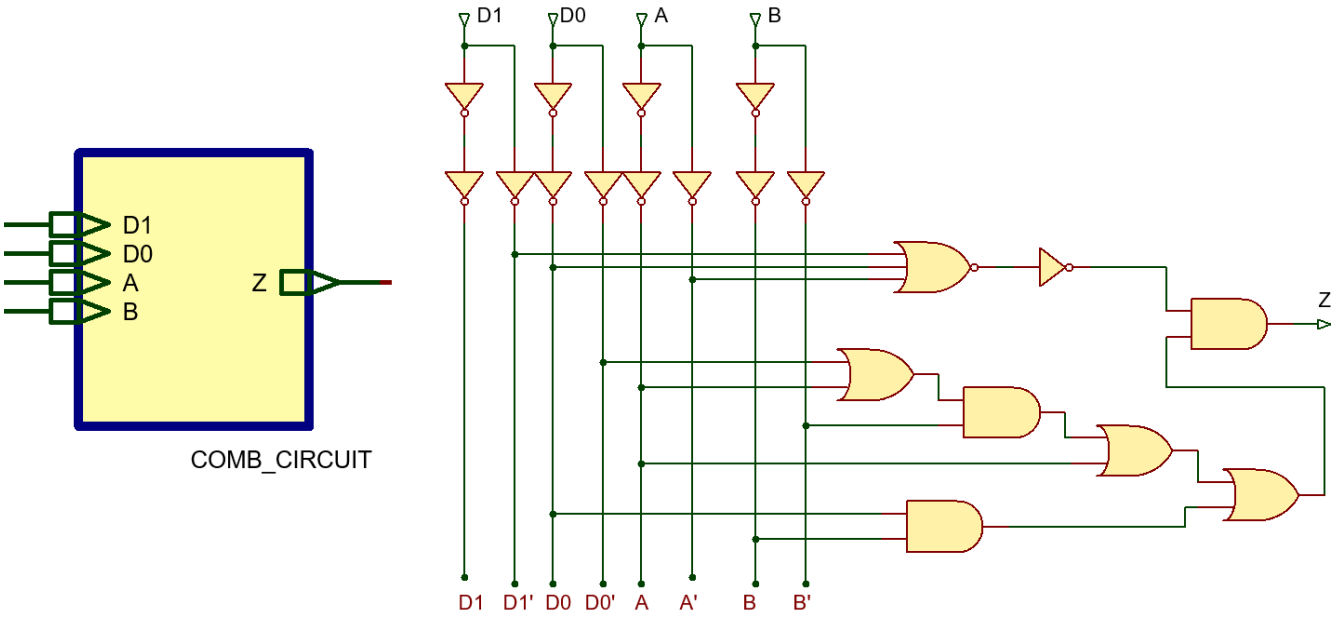


Fig. 2. Combinational circuit Z = *f*(D1, D0, A, B)

Problem 3 (4p)

For the 4-bit binary radix-2 to Johnson code converter in Fig. 3 with enable input, answer the following questions:

1. Complete the truth table. Obtain the canonical equations for J_7 and J_5.
2. If the circuit is solved completely using plan A, CMOS gates and canonical equations, calculate its propagation delay and maximum speed of operation.
3. Connect LED active-low at each circuit output (V_{AKQ} = 2.1 V). Calculate the limiting resistors to drive each LED with 700 µA in the worst-case scenario using CMOS logic.
4. Describe the schematic or flowchart to be able to translate the truth table into VHDL using plan B.

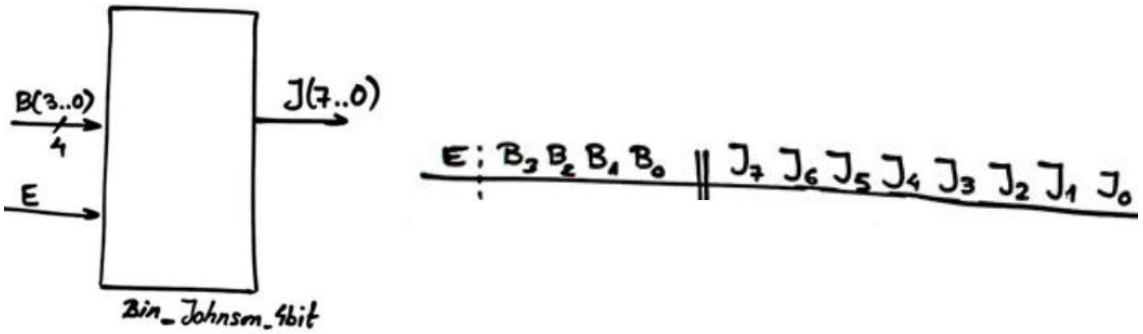


Fig. 3.

Problem 4 (4p)

For the 8-bit Johnson to binary radix-2 converter with enable input represented in in Fig. 4, answer the following questions:

1. Complete the truth table. Obtain the canonical equations for B_3 and B_1 indicating the terms of no interest as don't care values.
2. If the circuit is solved completely using plan A, LS-TTL gates and simplified equations SoP or PoS from Minilog, calculate its propagation delay and maximum speed of operation.
3. Connect LED active-high at each circuit output (V_{AKQ} = 1.9 V). Calculate the limiting resistors to drive each LED with 3.9 mA in the worst-case scenario using LS-TTL logic.
4. Describe the schematic or flowchart to be able to translate the truth table into VHDL using plan B.

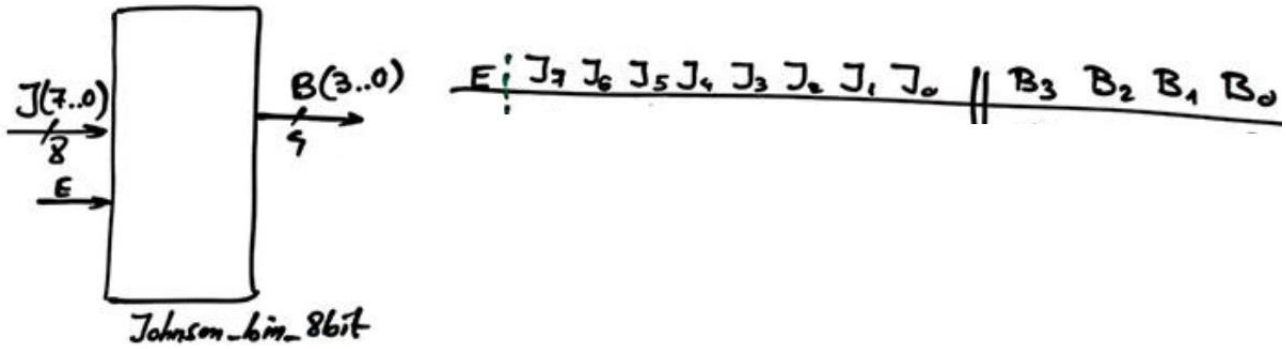


Fig. 4.

Problem 5 (4p)

For the 4-bit (nibble) shifter operator circuit represented in Fig. 5, controlled by shift-right (SR) and shift-left (SL) signals, answer the following questions:

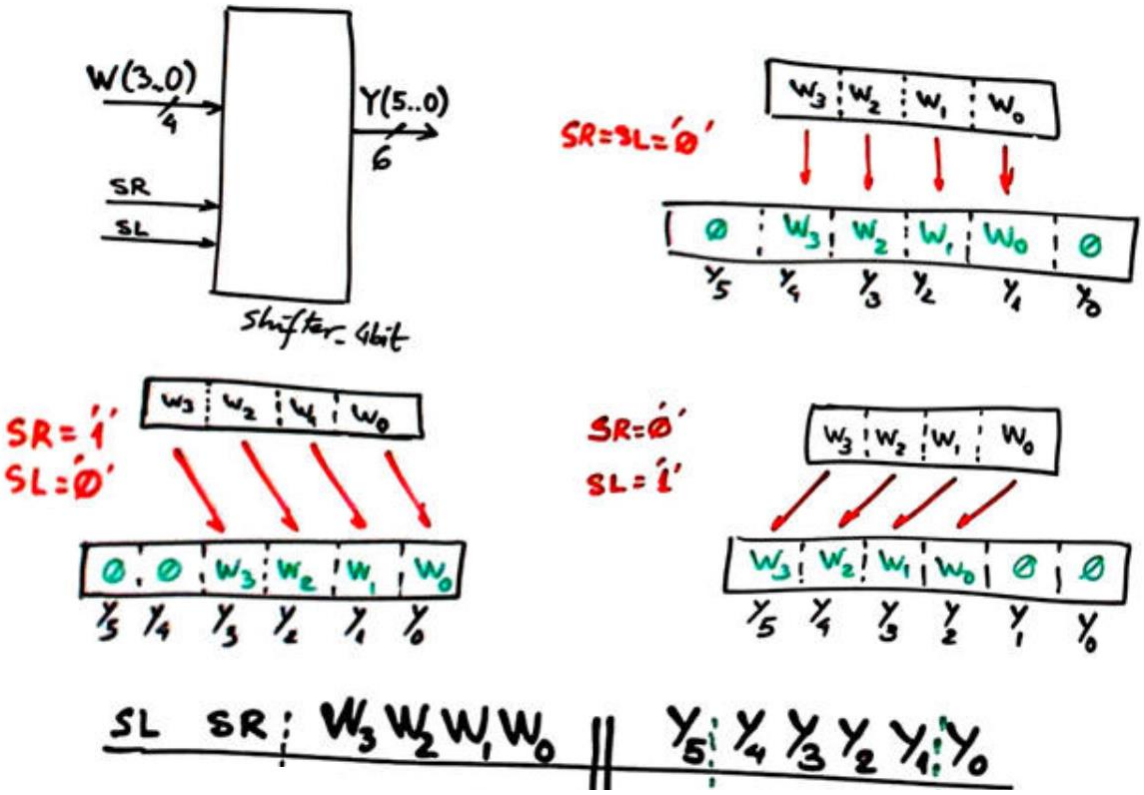


Fig. 5.

1. Complete its truth table indicating its four sections. Write the list of minterms of Y_3 and Y_2 when in shift-right mode. What combinations generate incomplete functions because they are of no interest?
2. If the circuit is solved completely using plan A, CMOS gates and simplified equations SoP or PoS from Minilog, calculate its propagation delay and maximum speed of operation.
3. Connect LED active-high at each circuit output (V_{AKQ} = 1.85 V). Calculate the limiting resistors to drive each LED with 350 µA in the worst-case scenario CMOS logic.
4. Describe the schematic or flowchart to be able to translate the truth table in VHDL using plan B.

Problem 6 (4p)

For the 2-digit multiplexed 7-segment display shown in Fig. 6, answer the following questions:

1. Complete the truth table. Obtain the canonical equations AN_1 and AN_0.
2. If the circuit is solved completely using plan A, LS-TTL gates and canonical equations, calculate its propagation delay and maximum speed of operation.
3. Calculate the limiting resistors to drive each LED (V_{AKQ} = 2.23 V) segment with 2.5 mA in the worst-case scenario using LS-TTL logic.
4. Describe the schematic or flowchart to be able to translate the truth table in VHDL using plan B.

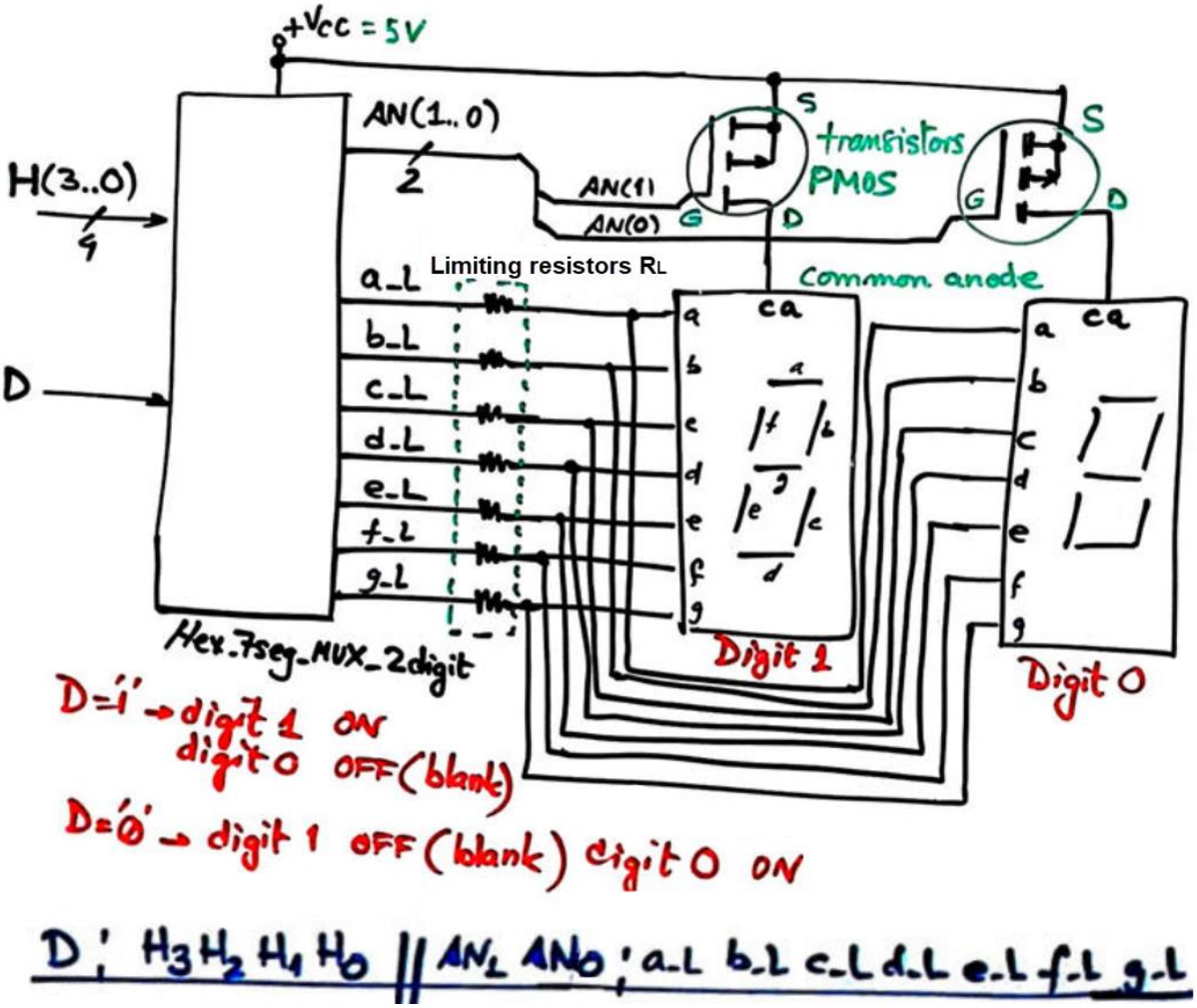
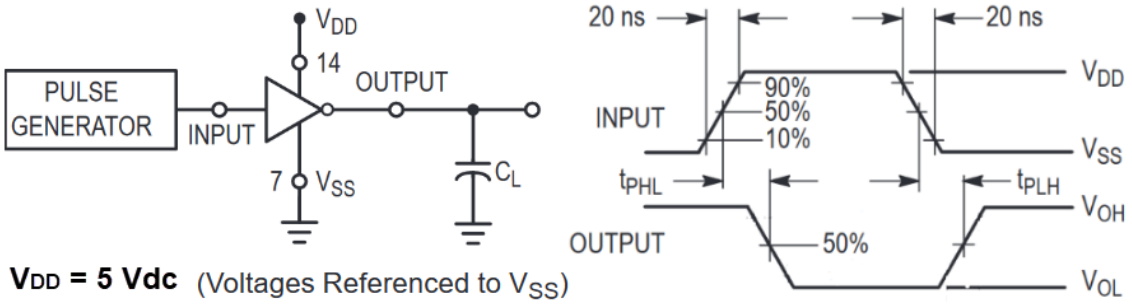


Fig. 6.

Fig. 7 shows the electrical characteristics of a single logic gate in classic CMOS and LS-TTL technologies.

$$P_S + P_{dyn} = I_{DDQ} \cdot V_{DD} + V_{DD}^2 \cdot C_L \cdot f$$

MC14069UB 	Symbol	25°C			Unit
		Min	Typ	Max	
Output Voltage V_{in} = V_{DD} "0" Level	V_{OL}	—	0	0.05	Vdc
V_{in} = 0 "1" Level	V_{OH}	4.95	5.0	—	Vdc
Input Voltage "0" Level (V_O = 4.5 Vdc)	V_{IL}	—	2.25	1.0	Vdc
"1" Level (V_O = 0.5 Vdc)	V_{IH}	4.0	2.75	—	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	– 2.4	– 4.2	—	mAdc
(V_{OH} = 4.6 Vdc)		– 0.51	– 0.88	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	0.51	0.88	—	mAdc
Input Current	I_{in}	—	±0.00001	± 0.1	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	5.0	7.5	pF
Quiescent Current (Per Gate)	I_{DD}	—	0.084	42	nAdc
Total Supply Current (C_L = 50 pF) (Dynamic plus Quiescent (Per Gate)	I_T	I_T = (0.3 µA/kHz) f + I_{DD}			µAdc
Propagation Delay Times (C_L = 50 pF) t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 20 ns	t_{PLH}, t_{PHL}	—	65	125	ns



V_{DD} = 5 Vdc (Voltages Referenced to V_{SS})

Fig. 7. Characteristics of a logic gate in CMOS technology

Fig. 8 shows the characteristics of a single logic gate in LS-TTL technology.

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA

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Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.2	2.4	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		3.6	6.6	mA

Symbol	Parameter C_L = 50 pF	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	4	15	ns

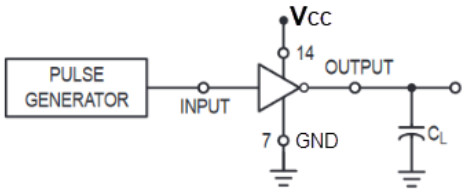

Fig. 8. Characteristics of a logic gate in LS-TTL technology

NOTE for all problems and questions: draw circuits, sketches or diagrams, explain as clear as possible what you do and how you are inventing circuits or processing calculations. Justify your results.