

Exam 1. Choose to solve only 10 of the 20 questions proposed (1p each question) **October 23, 2023**

Problem 1

1. Obtain the logic expression $G = f(A, B, C)$ of the circuit in Fig. 1. Translate it to VHDL as if you had to analyse the circuit using method III.
2. Calculate the circuit's worst-case propagation time and explain using a timing diagram what is the meaning of such concept. Calculate the circuit's maximum speed using schematics, instruments and timing diagrams. CMOS technology has the characteristics in Fig. 2.
3. Calculate the static power consumption. Calculate the dynamic power consumption imagining that all the gates are switching at maximum speed. Represent the transfer function and the noise voltage margins of a CMOS gate.
4. Simplify the circuit to obtain PoS or SoP equations.
5. Obtain the truth table of $G = f(A, B, C)$ and the corresponding canonical equations.
6. Invent a new circuit $G = f(A, B, C)$ using only NOR2 logic gates.

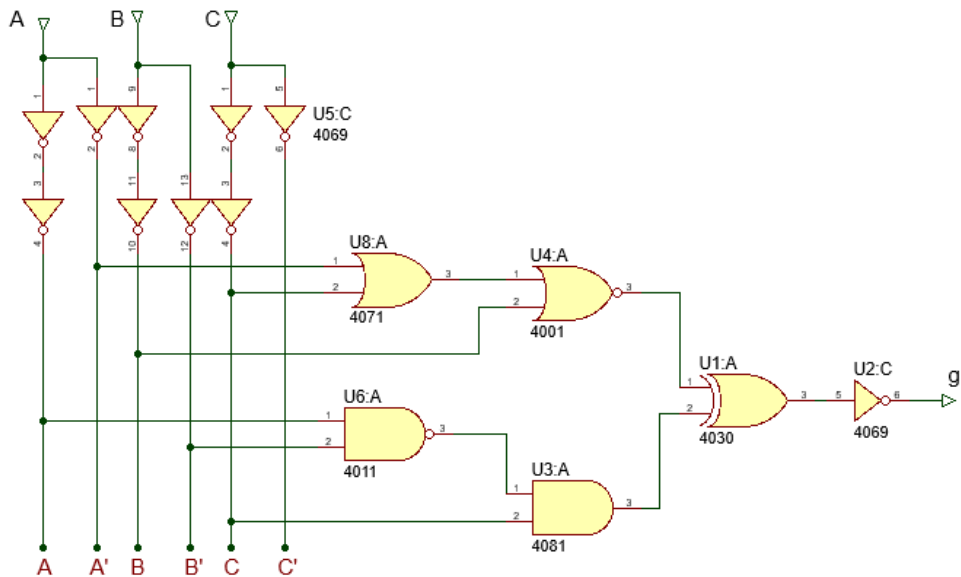


Fig. 1. Combinational circuit based on logic gates.

Electrical Characteristics – Dynamic

$T_A = 25^\circ\text{C}$; input $t_r, t_f = 20 \text{ ns}$; $C_L = 50 \text{ pF}$; $R_L = 200 \text{ k}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL} Propagation delay time	$V_{DD} (V) = 5$		55	110	ns

Electrical Characteristics – Static

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL} Low-level output voltage	$V_{IN} = 5 \text{ V}, V_{DD} = 5 \text{ V}$		0	0.05	V
V_{OH} High-level output voltage	$V_{IN} = 0 \text{ V}, V_{DD} = 5 \text{ V}$	4.95	5		V
V_{IL} Input low voltage	$V_O = 4.5 \text{ V}, V_{DD} = 5 \text{ V}$			1	V
V_{IH} Input high voltage	$V_O = 0.5 \text{ V}, V_{DD} = 5 \text{ V}$	4			V
I_{DDQ} Quiescent device current	$V_O = 0.5 \text{ V}, V_{DD} = 5 \text{ V}$		0.01	0.25	μA

$$P_S + P_{dyn} = I_{DDQ} \cdot V_{DD} + V_{DD}^2 \cdot C_L \cdot f$$

Fig. 2. CMOS technology characteristics for a single typical logic gate.

Problem 2

The Fig. 3 shows the symbol and an example of a functional simulation wave diagram of the *Sel_comp_8bit* comparator when $N = '0'$, and so, the data is unsigned in radix-2.

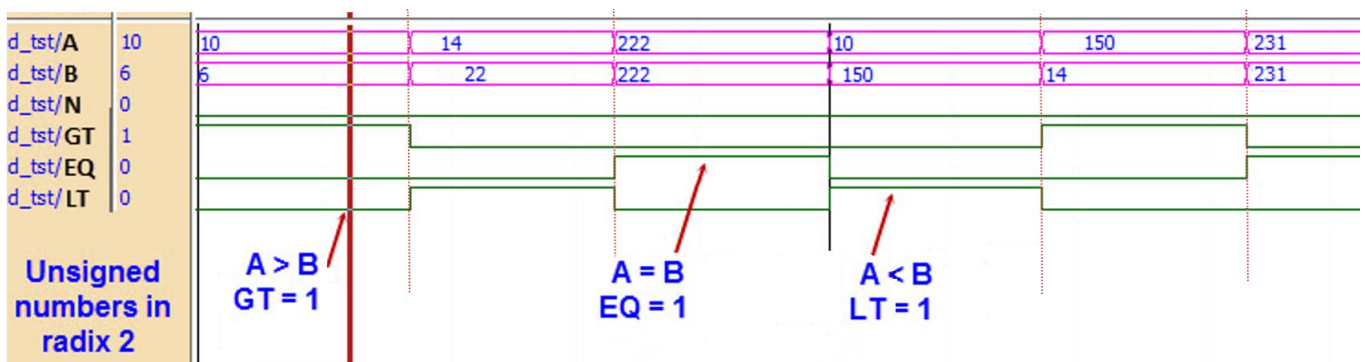
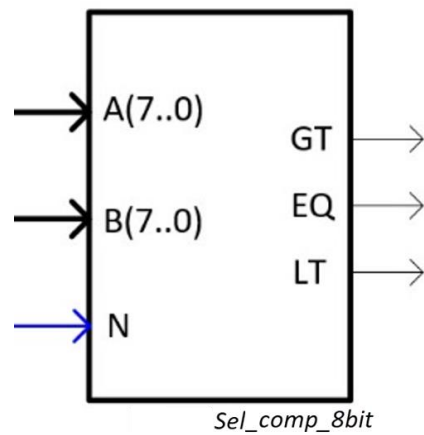


Fig. 3. Example wave diagram from a partial testbench simulation when $N = 0$.

- How long is the circuit's truth table? Write some values of the truth table using the input stimulus in Fig. 3 represented in '1' and '0' in radix-2 when $N = '0'$. What is the range of the operands?
- Draw a similar timing diagram and truth table deducing the new output values supposing that now $N = '1'$ and thus the same A and B input combinations in '0' and '1' represent integer numbers in two's complement. What is the range of the operands?
- Propose a plan C2 hierarchical internal design of the circuit in Fig. 3 based on simpler chips of the same kind. How many components will be necessary? How many VHDL files will contain this project?
- Draw the testbench schematic fixture. If in the testbench the time constant $Min_Pulse = 1.75 \mu s$, how long does it take to run the simulation of the complete truth table? If the internal component *Comp_1bit* is solved using plan A equations in 3-levels-of-gates, and the technology is the CMOS in Fig. 2, what is the minimum Min_Pulse value?

NOTE for all questions: explain what you do, how are you inventing the circuits and justify your results and calculations.

Problem 3

The equation in Fig. 4 represents a truth table which is going to be solved in VHDL using the plan B (behavioural) and the plan C2 (hierarchical based on components).

$$P = f(x_3, x_2, x_1, x_0) = \prod M(1, 2, 5, 7, 8, 10, 13, 15)$$

Fig. 4. Truth table of a 4-input combinational circuit named *Circuit_P*.

11. Solve the function **P** using a plan B, a behavioural approach. Represent a schematic or flowchart and explain how to translate it into VHDL. What resources are used when synthesising this circuit in an FPGA?
12. Solve the function **P** using the method of decoders (MoD).
13. Invent a decoder *Dec_4_16* using components of the same kind *Dec_2_4* and logic gates if necessary.
14. Solve the function **P** using the method of multiplexers (MoM) and a *MUX_4*.
15. Invent a *MUX_16* using components of the same kind (*MUX_4* and *MUX_2*) and logic gates if necessary.
16. Draw and calculate a circuit to drive a LED active-low connected at output **P** in the indicated bias point in Fig. 5. Use the chip technology in Fig. 2.

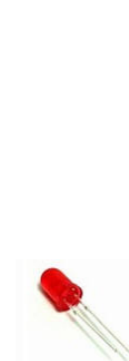
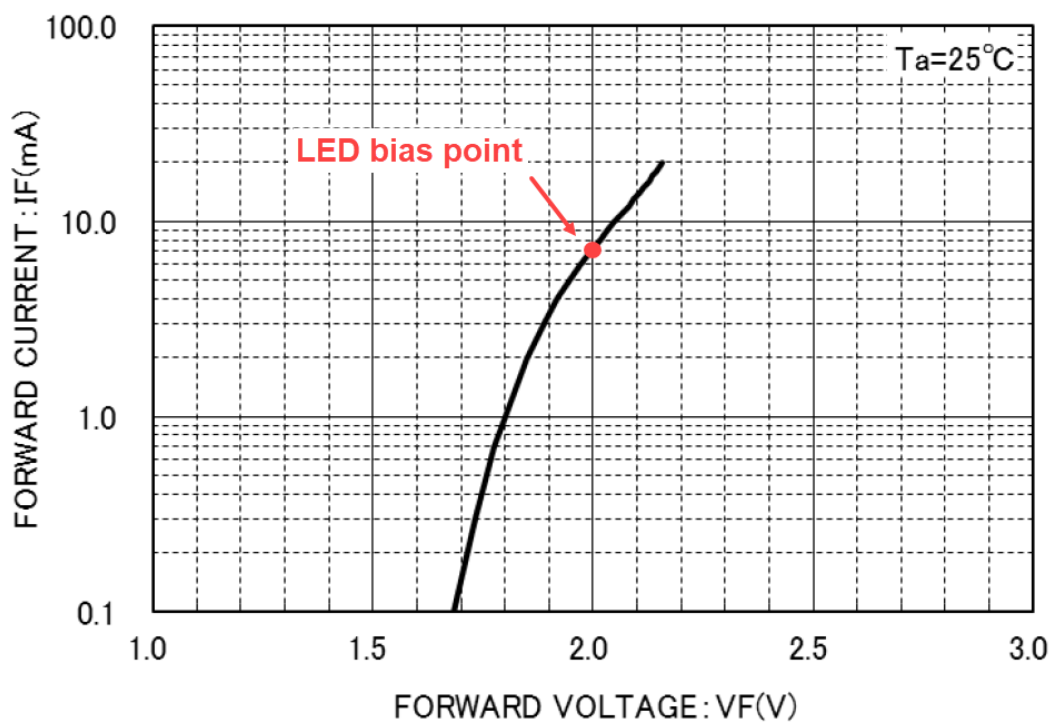


Fig. 5. Typical LED bias characteristics.

Problem 4

On the design an *Int_Add_subt_9bit* arithmetic circuit for 2C integer numbers.

17. Draw the circuit symbol and example truth table observing simulation results in Fig. 6 and considering the operands in 2C. Determine the range of the operands (A, B) and result (R). Perform using binary symbols ('0' and '1'), some operations for integers in binary two's complement to demonstrate the algorithm.

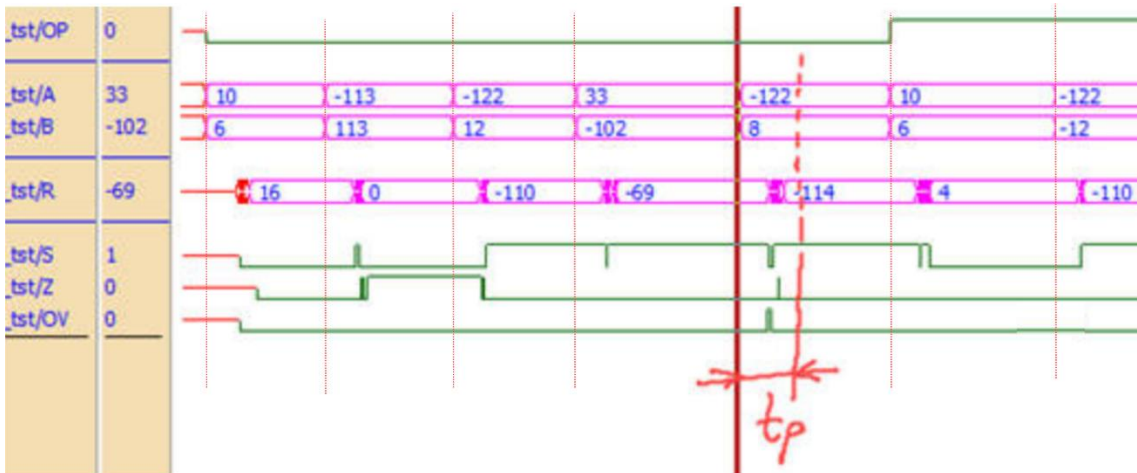


Fig. 6. Example of *Int_Add_Subt_9bit* simulation wave results.

18. Using Fig. 6 as a reference, draw an ideal timing diagram adding some new operands in 2C to demonstrate as well how the circuit overflows (OV = '1'). Perform the arithmetic to calculate results using binary symbols ('0' and '1'). What is the OV detection algorithm or function?
19. Propose and draw a hierarchical plan C2 internal circuit based on binary radix-2 adder components such the classic chip 74LS283 represented in Fig. 7.

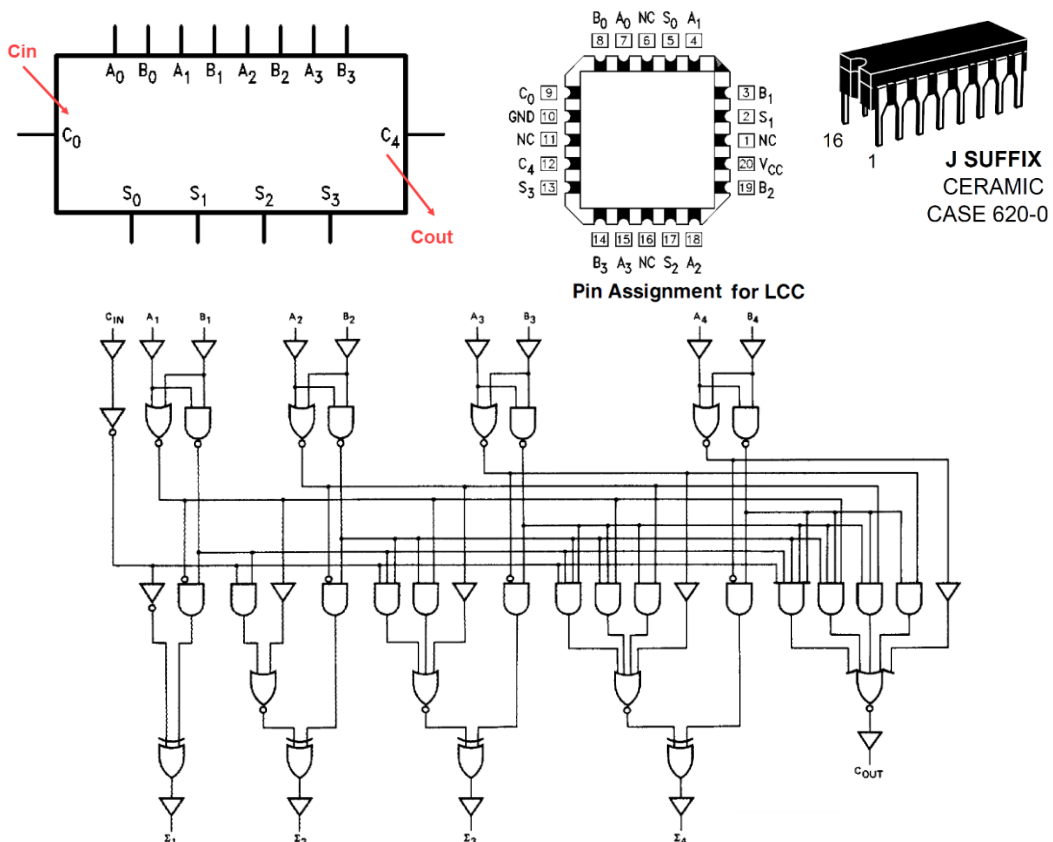


Fig. 7. Commercial chip 74LS283 and its RTL circuit (*Adder_4bit*).

20. Explain what is the parameter t_p in Fig. 6 and how and using which tools such simulation results are obtained. If the technology 74LS has a $t_{p(1gate)} = 3.6$ ns, calculate and explain the maximum operating speed of the *Int_Add_Subt_9bit*.