Problem 1

1.

x_3	x_2	x_1	x_0	K
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	X
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	X
1	0	1	1	0
1	1	0	0	0
1	1	0	1	X
1	1	1	0	1
1	1	1	1	0

$K = m_0 + m_1 + m_4 + m_7 + m_{11} + m_{14}$

$K = (m_0 + m_1 + m_4 + m_7 + m_{11} + m_{14})'' = (m_0' \cdot m_1' \cdot m_4' \cdot m_7' \cdot m_{11}' \cdot m_{14}')'$ only NAND

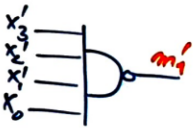
$K = (x_3' x_2' x_1' x_0' + x_3' x_2' x_1 x_0 + x_3' x_2 x_1' x_0' + x_3' x_2 x_1 x_0 + x_3 x_2' x_1 x_0 + x_3 x_2 x_1 x_0')''$

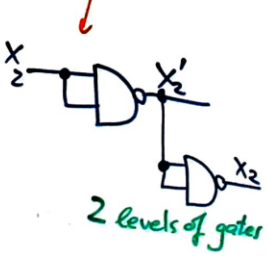
$K = ((x_3' \cdot x_2' \cdot x_1' x_0)' \cdot (x_3' x_2' x_1' \cdot x_0)' \cdot (x_3' x_2 x_1' x_0')' \cdot (x_3' x_2 x_1 x_0)' \cdot (x_3 x_2' x_1 x_0) \cdot (x_3 x_2 x_1 x_0')')'$

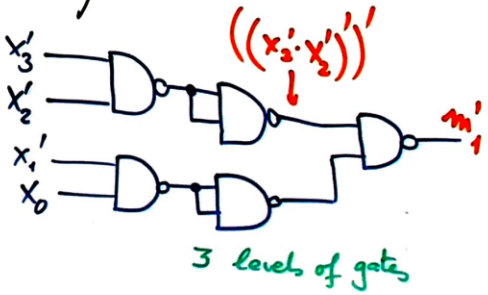
m_1'

$m_1' = ((x_3' \cdot x_2')'' \cdot (x_1' \cdot x_0)'')'$

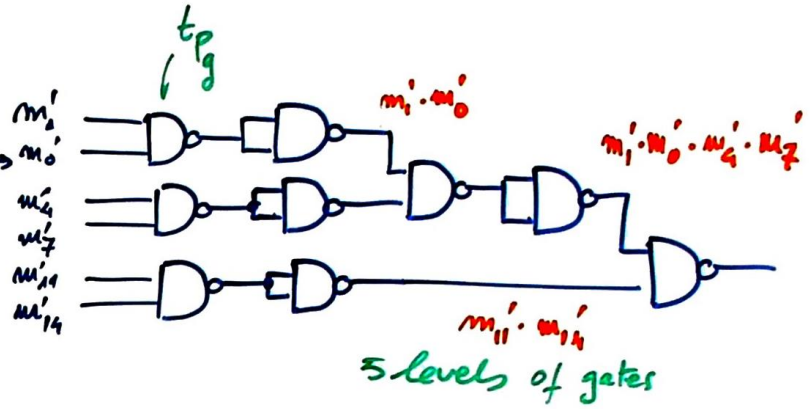
$m_1' = (((x_3' \cdot x_2')')' \cdot ((x_1' \cdot x_0)')')'$



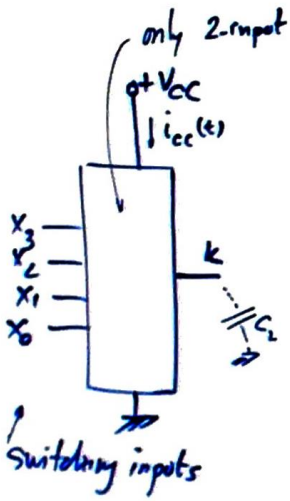




Final 6-input NAND



2. We can imagine the circuit driven with stimulus that make all internal gates switching



10 gate levels

$t_p = 10 \cdot t_{p_g} = 120\ ns$

$P_D = V_{CC} \cdot I_{CC} + V_{DD}^2 \cdot C_L \cdot f$

$P_s \quad + \quad P_{dyn}$

30
+ 8
9
47 gates

- We assume all gates switch at f and all gates associated to a $C_L = C_{pd}$

$$f_{max} \leq \frac{1}{2 \cdot t_p} = 4.17\ MHz$$

$P_{dyn} = 47 \cdot 5V^2 \cdot 12pF \cdot 4.17\ MHz = 68.8\ mW$

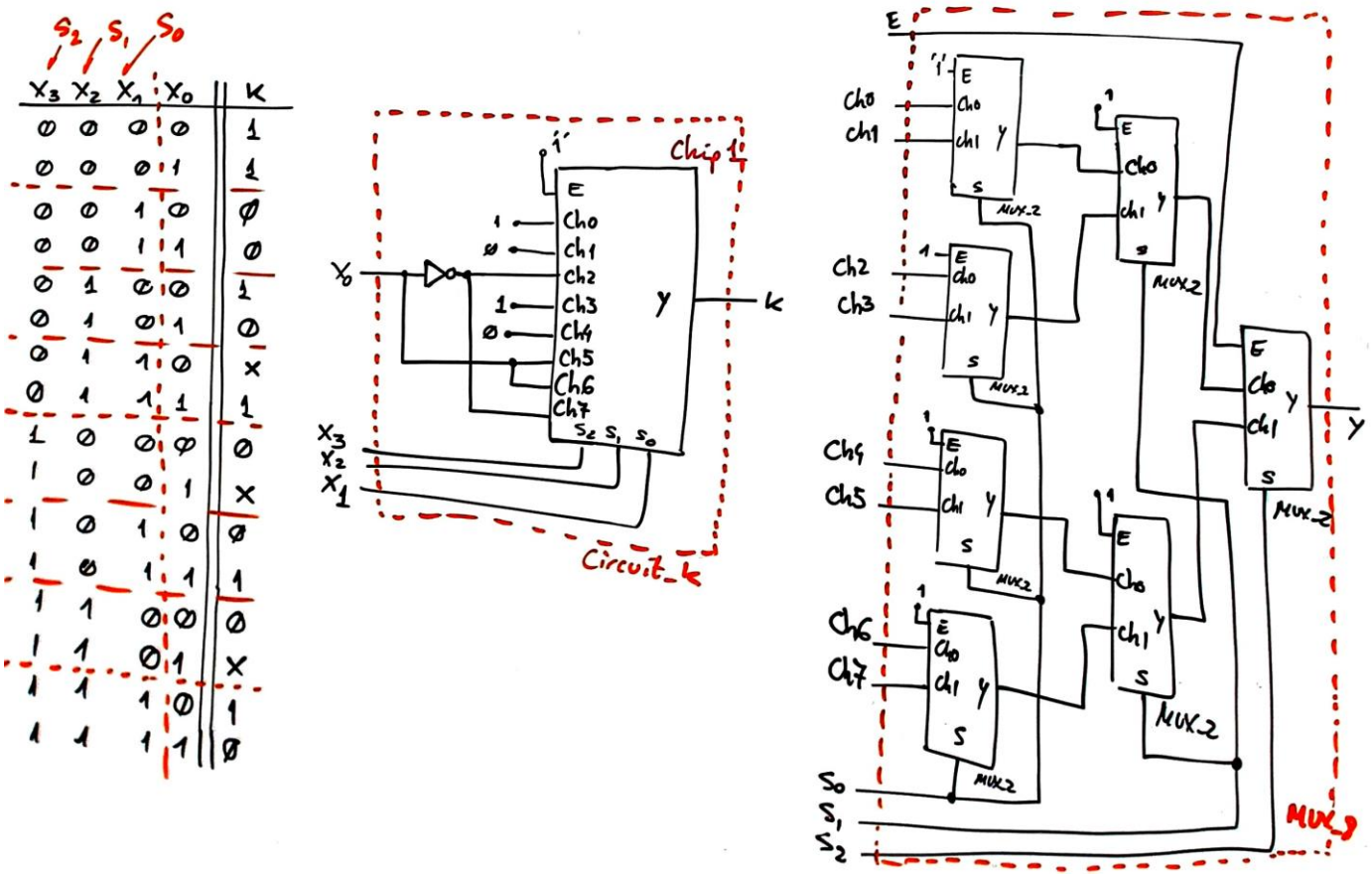
$P_s = 5V \cdot 20\mu A \cdot 47 = 4.7\ mW$ (47: number of NAND)

$P_D = 63.5\ mW$

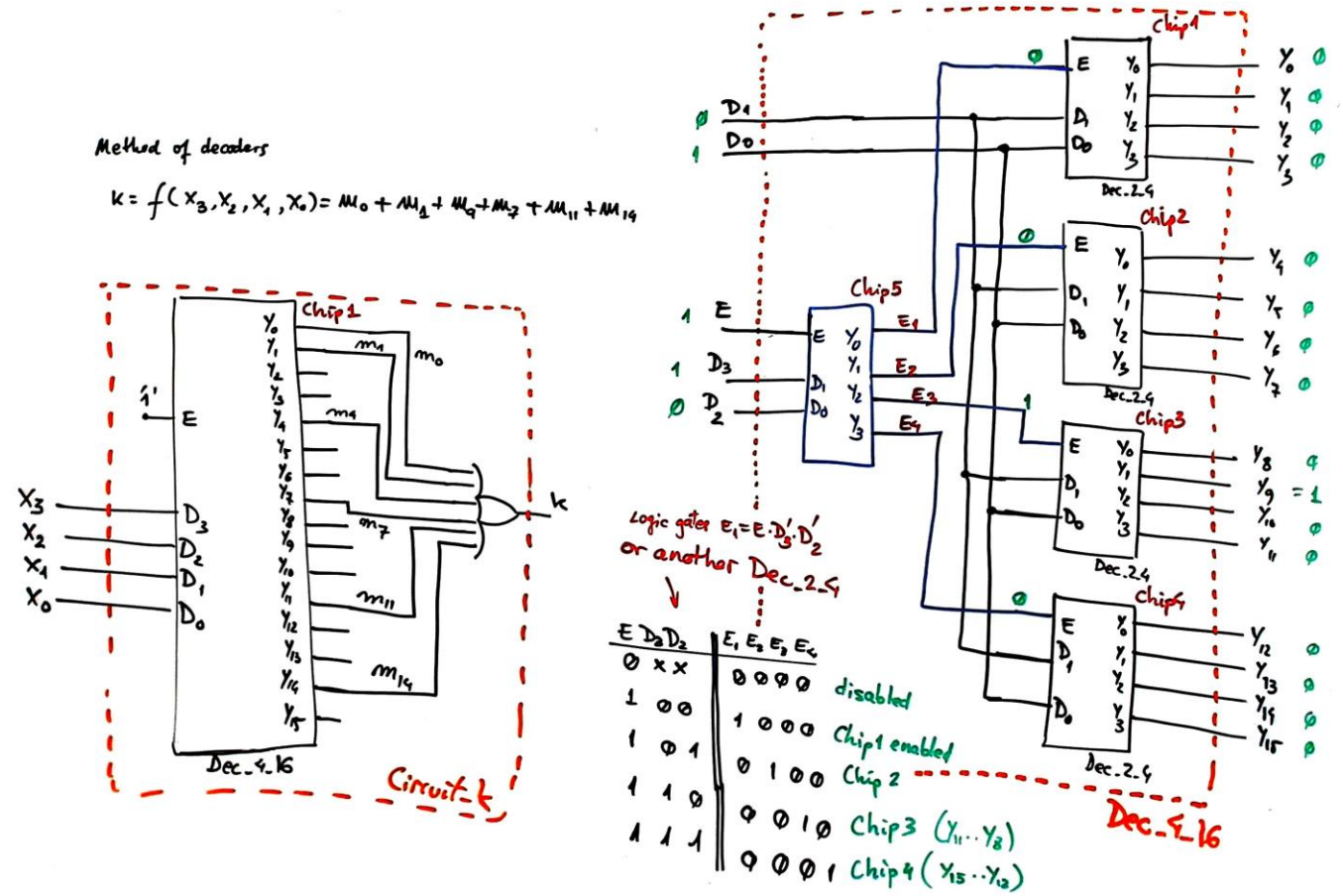
3.

Min_Pulse minimum value for simulations or laboratory experimentation cannot be lower than t_P. If *Min_Pulse* < t_P digital outputs are never reaching stable digital values V_{OH} and V_{OL}.

4.

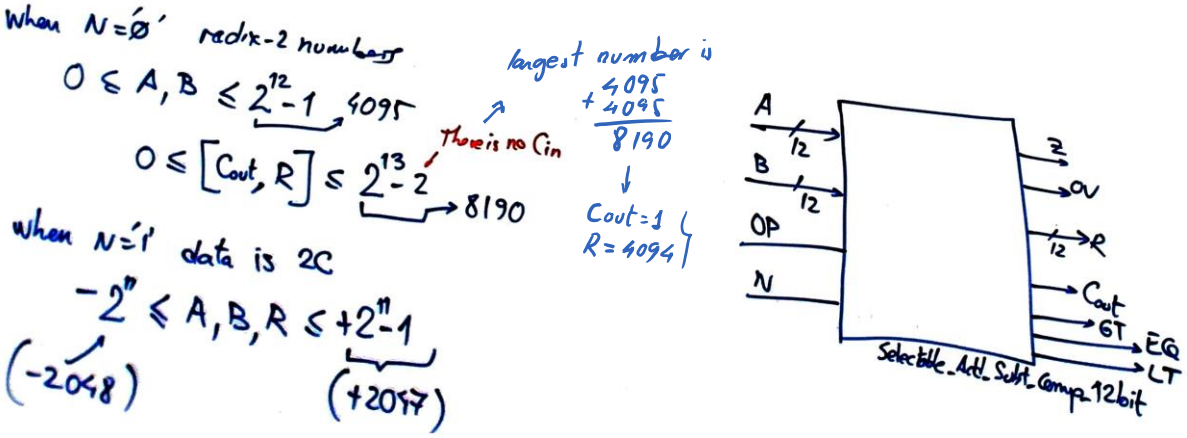

S2 S1 S0
X3 X2 X1 X0 K
Chip 1
Circuit_k
MUX_2
MUX_3

5.

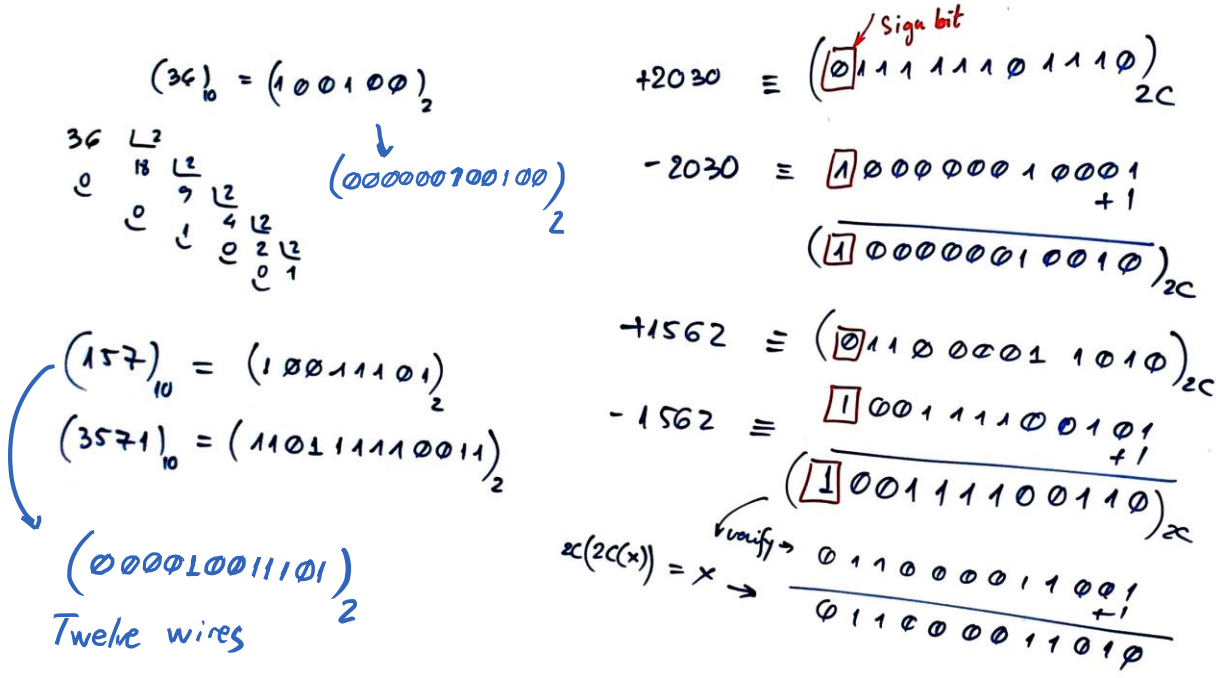

Method of decoders
k = f(X3, X2, X1, X0) = m0 + m1 + m4 + m7 + m11 + m14
Chip1
Chip2
Chip3
Chip4
Chip5
Dec_4_16
Dec_2_4
Circuit_k
Logic gate E1 = E·D3'·D2'
or another Dec_2_4
E D3 D2 | E1 E2 E3 E4
0 x x | 0 0 0 0 disabled
1 0 0 | 1 0 0 0 Chip1 enabled
1 0 1 | 0 1 0 0 Chip 2
1 1 0 | 0 0 1 0 Chip3 (Y11..Y8)
1 1 1 | 0 0 0 1 Chip4 (Y15..Y12)

Problem 2

6.



7. Use the calculator to calculate radix 2 numbers. Data size is 12 bit. Apply the 2C convention for integers.

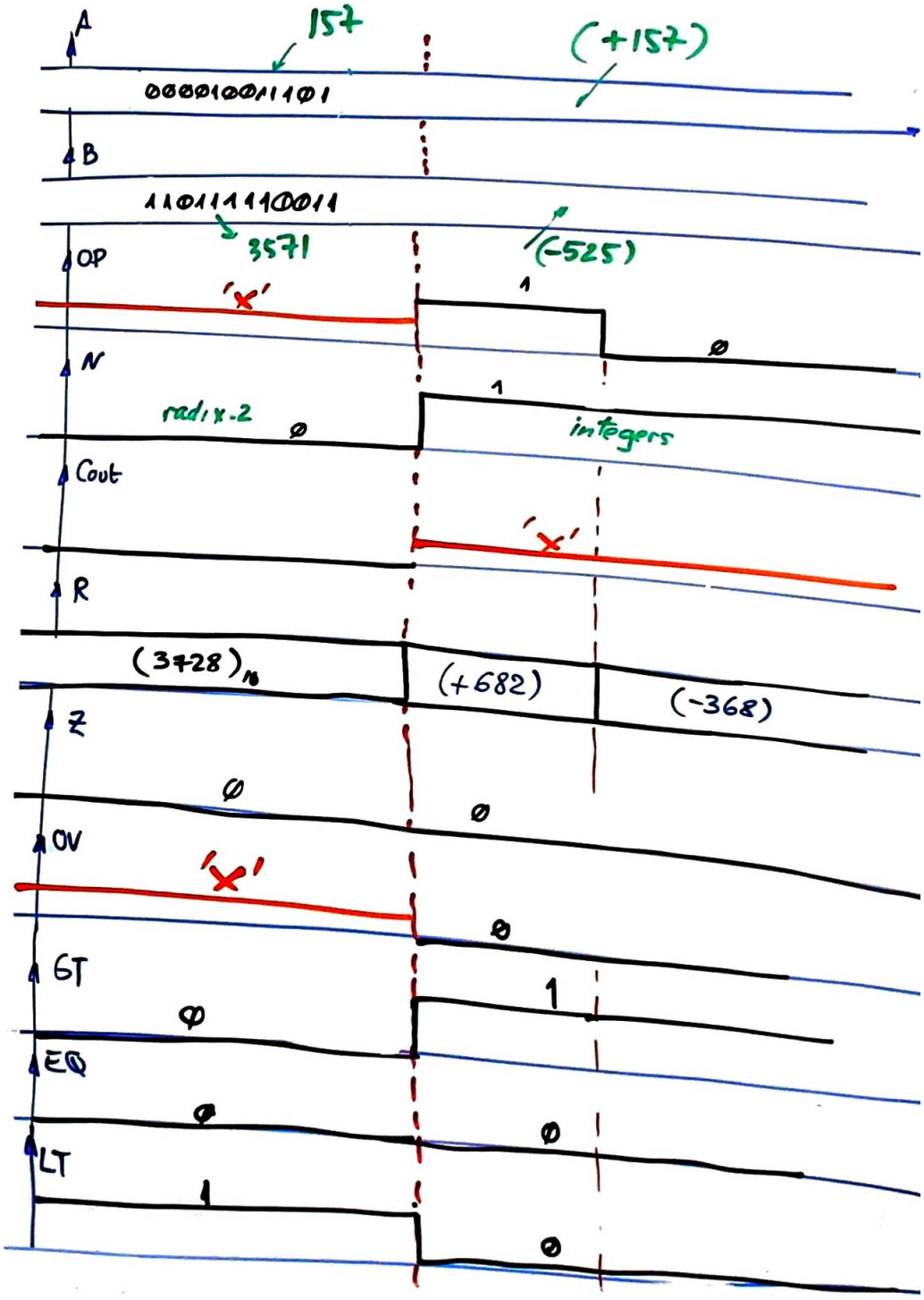


8. *Min_Pulse* = 105 ns

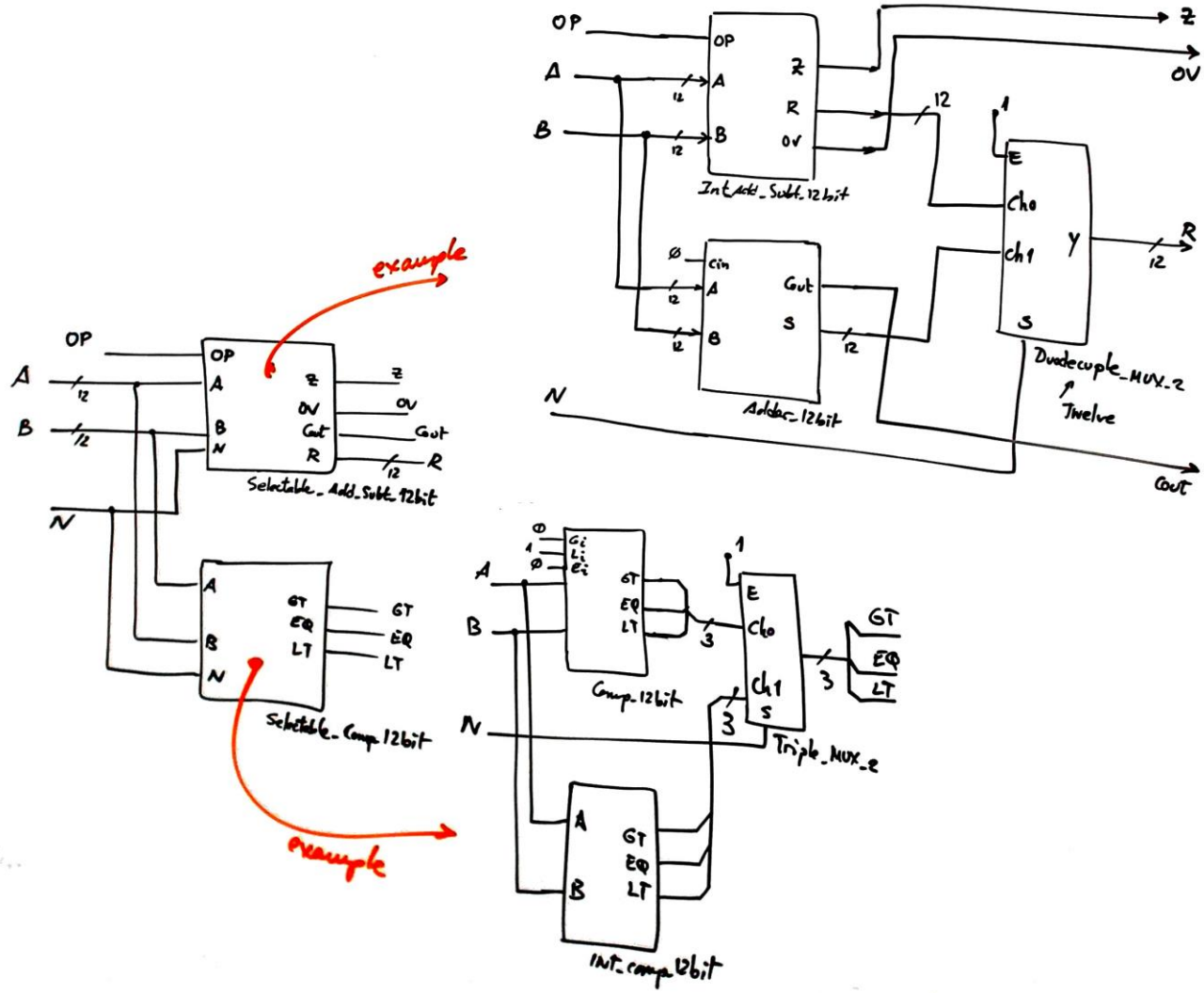
$2^{12} \cdot 2^{12} \cdot 2^{1} \cdot 2^{1} = 2^{26} =$ 67108864 combinations

automating the test bench for generating all test vectors, it will take:

$$\text{run time} = 2^{26} \cdot \text{Min\_Pulse} = 7.05\,s$$



9. Plan C2 allows top-down architecture organisation using simpler components. In a second phase, circuits can be optimised reducing the number of components and multiplexers.



10. Solved for 8-bits at P4: https://digsys.upc.edu/csd/P04/P4.html

11. Solved at this P3 tutorial: https://digsys.upc.edu/csd/P03/Comp_4bitC2/Comp_4bit.html

12. EQ is a bitwise XOR operation followed by a 12-input NOR gate.

First level of gates:
$K_{11} = A_{11} \oplus B_{11}$; $K_{10} = A_{10} \oplus B_{10}$; ….$K_0 = A_0 \oplus B_0$

Then a second level → NOR
$EQ = (K_{11} + K_{10} + \cdots + K_1 + K_0)'$

If the numbers are identical, all XOR outputs are 0, and so, EQ = 1
If any $A_i \neq B_i$ → $K_i = 1$, and thus → EQ = 0

13. Solved for example in this P2 plan A tutorial on Adder_1bit:
https://digsys.upc.edu/csd/P03/Adder_1bit_A/Adder_1bit_A.html

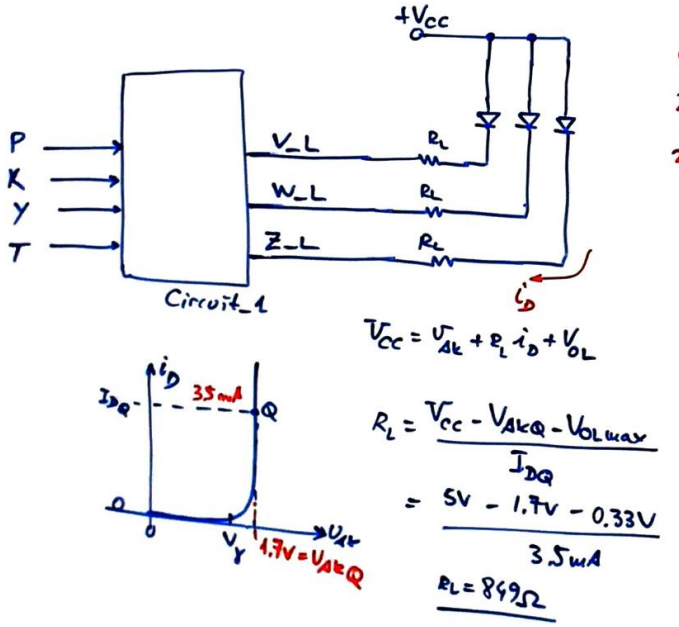
Ai	Bi	Ci	Co	So
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$Co = f(Ai, Bi, Ci) = \prod M(0,1,2,4)$$

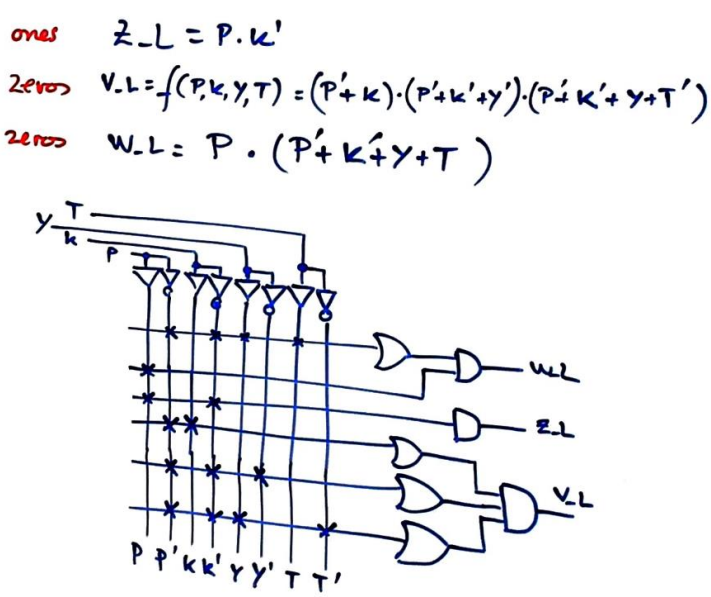
$$So = f(Ai, Bi, Ci) = \prod M(0,3,5,6)$$

Problem 3

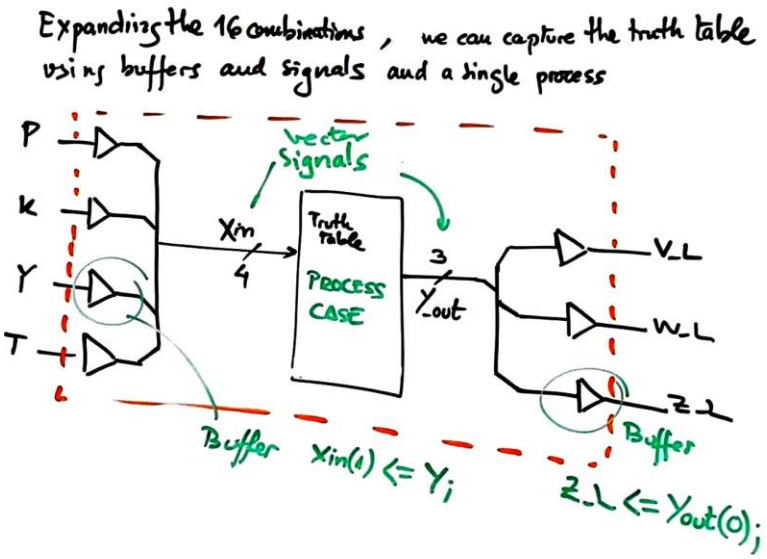
14.



15.



16.




```
PROCESS (Xin)
    CASE Xin IS
        WHEN "0000" =>
            Yout <= "100";
        WHEN "0001" =>
            Yout <= "100";
            ⋮
        WHEN "1110" => Yout <= "010";
        WHEN others =>
            Yout <= "010";
    END CASE;
END PROCESS;
```