UPC. EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). Grades will be available online by November 14. Questions about the exam at office time.

Midterm exam. **November 7, 2022**

Problem 1 (3p)

1. Solve the function K in Fig. 1 using only 2-input NAND.

$$K = f(X_3, X_2, X_1, X_0) = \sum m(0,1,4,7,11,14) + \sum d(6,9,13)$$

Fig. 1. Truth table of *Circuit_K*. ('*d*' are don't care terms).

2. *Circuit_K* invented in **1** will be implemented using a classic technology HCT (High Speed CMOS with TTL outputs) with the characteristics shown in Fig. 2. Deduce and explain the maximum speed of computing and estimate the total power consumption at such frequency.

3. What is the minimum value of *Min_Pulse* if we intent to run gate-level simulations?

Symbol	Parameter	Test Conditions V_{CC} = 5 V	T_A = -40°C to +85°C		Unit
			Min	Max	
V_{IH}	High-level Input Voltage		2.0		V
V_{IL}	Low-level Input Voltage			0.8	V
V_{OH}	High-level Output Voltage	I_{OH} = -20μA	4.4		V
		I_{OH} = -4mA	3.84		
V_{OL}	Low-level Output Voltage	I_{OL} = 20μA		0.1	V
		I_{OL} = 4.0mA		0.33	
I_{CC}	Supply Current	V_I = GND or V_{CC}		20	μA

Power Dissipation Capacitance per Gate	Typ	Unit
C_L	12	pF

Symbol	Parameter	Typ	Unit
t_{Pg}	Propagation Delay	12	ns

$$P_{gate} = P_S + P_{dyn} = I_{CCQ} \cdot V_{CC} + V_{CC}^2 \cdot C_L \cdot f$$

Fig. 2. Technology characteristics of HCT logic gates (adapted from 74HCT00 datasheet).

4. Invent *Circuit_K* using the method of multiplexers with a *MUX_8*. Solve the *MUX_8* expanding only *MUX_2* and logic if necessary. How many VHDL files will this project contain?

5. Firstly, invent *Circuit_K* using the method of decoders. Secondly, solve your decoder expanding *Dec_2_4* and logic if necessary.

Problem 2 (4p)

6. The truth table in Fig. 3 represents a *Selectable_Add_Subt_Comp_12bit* arithmetic circuit for operating with both integer (**N** = 1) and radix-2 (**N** = 0) numbers. Draw its symbol. Find the range of input and output data.

N	OP	A	B	C_{out}	R	OV	Z	GT	EQ	LT
0	x	36	157	0	193	x	0	0	0	1
0	x	3571	3571	1	3046	x	0	0	1	0
1	0	(+2030)	(-1562)	x	(+468)	0	0	1	0	0
1	1	(-2030)	(-2030)	x	0	0	1	0	1	0
1	0	(-2030)	(-2030)	x	x	1	0	0	1	0
1	1	(+1562)	(-2030)	x	x	1	0	1	0	0
1	0	(-2030)	(+1562)	x	(-468)	0	0	0	0	1

Fig. 3. Truth table of the arithmetic circuit *Selectable_Add_Subt_Comp_12bit*

7. Convert the signed and unsigned numbers in Fig. 3 into binary.

8. Draw an example of timing diagram (use the Fig. 4 template). Supposing *Min_Pulse* = 105 ns calculate how long does it take to test all the truth table of *Selectable_Add_Subt_Comp_12bit*.

9. Design the *Selectable_Add_Subt_Comp_12bit* circuit using components.

10. Propose an internal circuit for the *Int_Add_Subt_12bit* using components.

11. Design a *Comp_4bit* using *Comp_1bit.*

12. Design the output EQ using XOR gates.

13. Design an *Adder_1bit* using maxterms.

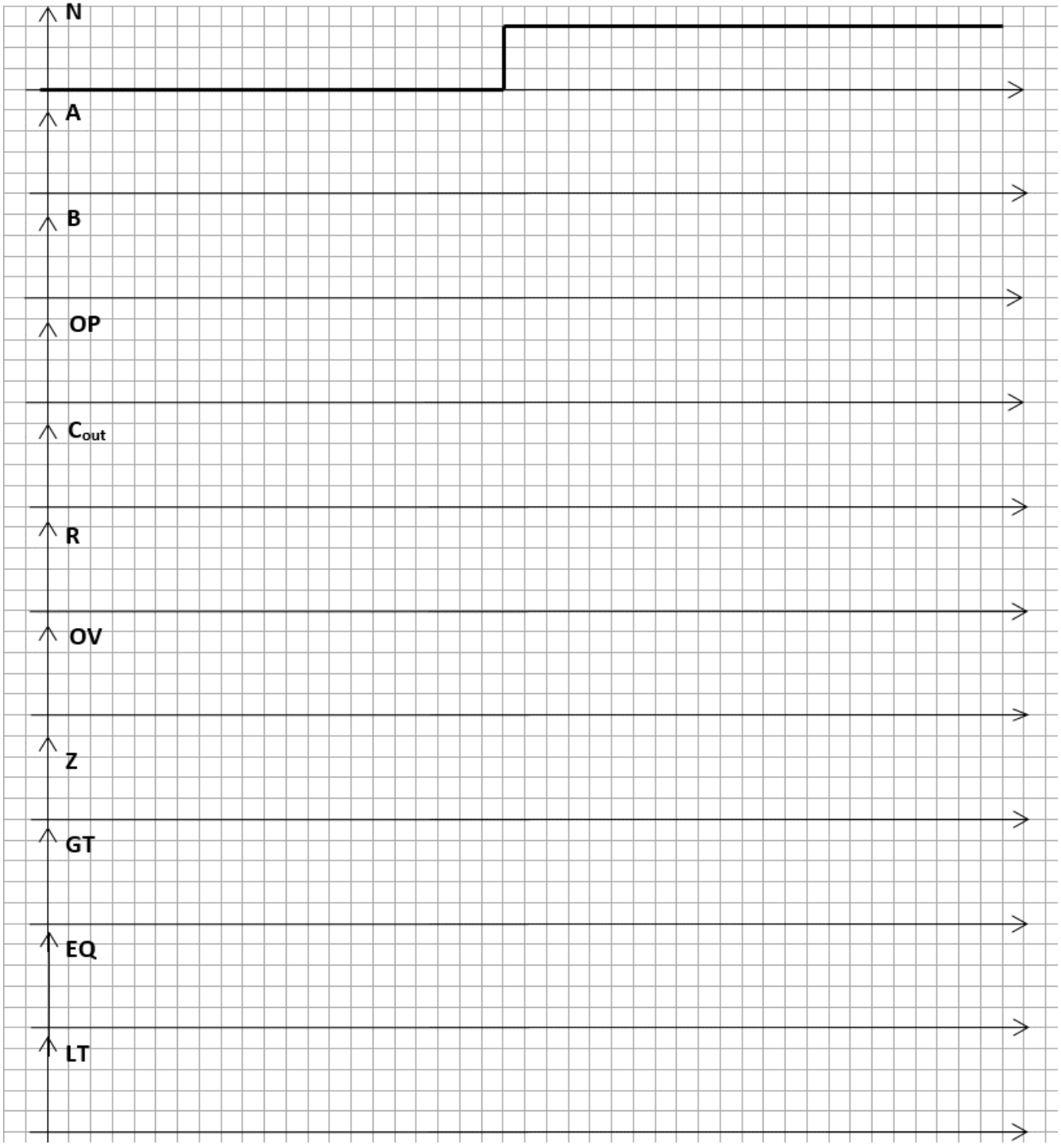

Fig. 4. Waveform template for representing the timing diagram in question **8**.

Problem 3 (3p)

14. Draw the symbol of the circuit represented by the truth table in Fig. 5 and calculate the limiting resistors to drive active-low LEDs (V_{AKQ} = 1.7 V, I_{DQ} = 3.5 mA) connected at the outputs supposing the electrical characteristics in Fig. 2.

P	K	Y	T	V_L	W_L	Z_L
0	x	x	x	1	0	0
1	0	x	x	0	x	1
1	1	1	x	0	1	0
1	1	0	1	0	1	0
1	1	0	0	1	0	0

Fig. 5. Truth table of a combinational circuit named *Circuit_1*.

15. Write the *Circuit_1* equations using PoS or SoP and draw the logic circuit.

16. Plan *Circuit_1* drawing a flowchart or schematic using plan B. Translate the main details to VHDL.