

Midterm exam.

April 19, 2022

Problem 1.

(5p)

1. Draw the symbol and an example of timing diagram for the combinational circuit *Circuit\_1* with the truth table represented in Fig. 1. Use a *Min\_Pulse* time constant of 15.24 μs and calculate how long it takes to run a VHDL testbench simulation to verify all the circuit. Indicate a possible application of this digital circuit.

B <sub>1</sub>	B <sub>0</sub>	A <sub>1</sub>	A <sub>0</sub>	R <sub>3</sub>	R <sub>2</sub>	R <sub>1</sub>	R <sub>0</sub>
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Fig. 1  
Truth table of a combinational circuit named Circuit\_1.

2. Express  $R_2 = g(B_1, B_0, A_1, A_0)$  as a product of maxterms and  $R_1 = f(B_1, B_0, A_1, A_0)$  as a sum of minterms and draw the equivalent circuits.
3. Simplify  $R_0$  using Boole's algebra and draw the logic circuit.
4. Implement the output  $R_3$  using only 2-input NOR logic gates and draw the circuit.
5. The circuit invented in the previous sections 2, 3, and 4 will be implemented using a classic technology ALS-TTL (Advanced Low Power Schottky) with the characteristics shown in Fig. 2. Deduce and explain the maximum speed of computing.
6. The circuit invented in the previous sections 2, 3, and 4, will be implemented using a classic technology ALS with the characteristics shown in Fig. 2. Deduce and explain the power consumption when powered at 5 V. Assume that the current consumption of a single logic gate is  $I_{CC} = (I_{CCH} + I_{CCL})/2$ .
7. Draw the schematic and calculate the limiting resistors to drive LEDs ( $V_{AKQ} = 2.1$  V,  $I_{DQ} = 9$  mA) active-high connected at the outputs.
8. Implement the circuit using plan C2 based on the method of decoders (MoD) and explain how many VHDL files the project contains.
9. Implement the circuit for output  $R_1$  using plan C2 based on the method of multiplexers (MoM) and a MUX\_2. Explain how many VHDL files the project contains.
10. Invent and plan the circuit for the output  $R_0$  using plan B (behavioural).

PARAMETER	SN74ALS04B			UNIT
	MIN	TYP	MAX	
V <sub>IK</sub>			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> - 2			V
V <sub>OL</sub>	0.25		0.4	V
	0.35		0.5	
I <sub>I</sub>	0.1			mA
I <sub>IH</sub>	20			μA
I <sub>IL</sub>	-0.1			mA
I <sub>O#</sub>	-30	-112		mA
I <sub>CCH</sub>	0.65		1.1	mA
I <sub>CCL</sub>	2.9		4.2	mA

		SN74ALS04B			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage	0.8			V
I <sub>OH</sub>	High-level output current	-0.4			mA
I <sub>OL</sub>	Low-level output current	8			mA
T <sub>A</sub>	Operating free-air temperature	0	70		°C

Fig. 2  
Technology characteristic for the logic family ALS-TTL

	MIN	MAX	ns
t <sub>PLH</sub>	3	11	
t <sub>PHL</sub>	2	8	

**Problem 2.**

(5p)

1. Draw the symbol and the hierarchical internal schematics (plan C2) of a 7-bit two's complement (2C) adder/subtractor (*Int\_Add\_Subt\_7bit*) for integer numbers. Name all the VHDL source files and explain their function. (1p)
2. Determine the range of the operands **A**, **B** and the result **R**. Explain how the overflow (**OV**) flag works and how its logic circuit and truth table can be inferred. (0.5p)
3. Perform the following operations in binary using the two's complement (2C) **7-bit** adder/subtractor from previous section 1). Check the result and deduce the **Z** (zero) and **OV** flags. (1p)

<b>a)</b>	$(+41)_{10}$	+	$(1001010)_{2C}$
<b>b)</b>	$(0110110)_{2C}$	-	$(-55)_{10}$
<b>c)</b>	$(+18)_{10}$	+	$(1101110)_{2C}$
<b>d)</b>	$(-29)_{10}$	-	$(0110110)_{2C}$

4. Represent the previous operations in a timing diagram and translate it (only the stimulus section) to a VHDL test bench process using a constant *Min\_Pulse* = 10.5  $\mu$ s. Furthermore, calculate how long it takes to run a testbench for simulating not only the four previous operations, but all the circuit's truth table. (0.5p)
5. Determine the maximum speed of operation of the 7-bit 2C adder/subtractor designed in section 1) if synthesised in an Altera MAX7128S CPLD device. The propagation delay of a logic gate in this technology is 2 ns. Justify your calculations. (1p)
6. Deduce the logic function and the corresponding circuit to add the new feature of equality (**EQ**) detection. This is a flag or indicator that goes high when the operands **A = B**. (0.5p)
7. Using the *Int\_Add\_Subt\_7bit* and other circuits, invent a 7-bit arithmetic and logic unit (ALU) capable of performing the following operations: (0.5p)

<b>S(1..0)</b>		
0		A + B
1		A - B
2		A <b>nand</b> B
3		A <b>xor</b> B