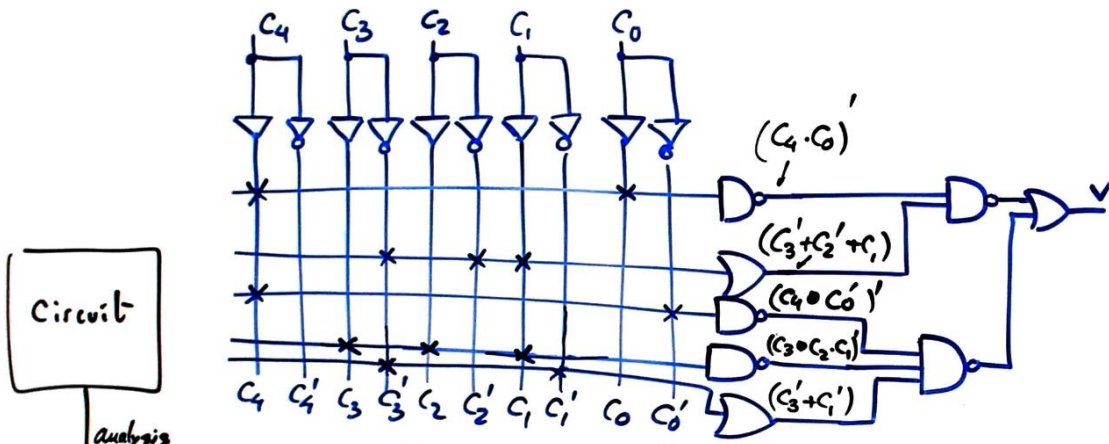


Problem 1



Circuit

analysis

Circuit equation

$$V = f(C_4, C_3, C_2, C_1, C_0) =$$

$$V = ((C_4 \cdot C_0)' \cdot (C_3 + C_2 + C_1))' + ((C_4 \cdot C_0)' \cdot (C_3 \cdot C_2 \cdot C_1)' \cdot (C_3 + C_1)')$$

Simplify using algebra

SoP

$$V = (C_4 \cdot C_0)'' + (C_3 + C_2 + C_1)' + (C_4 \cdot C_0)'' + (C_3 \cdot C_2 \cdot C_1)'' + (C_3 + C_1)'$$

$$= C_4 \cdot C_0 + C_3 \cdot C_2 \cdot C_1' + C_4 \cdot C_0' + C_3 \cdot C_2 \cdot C_1 + C_3 \cdot C_1$$

$$= C_4(C_0 + C_0') + C_3 \cdot C_2(C_1' + C_1) + C_3 \cdot C_1$$

②

$$V = C_4 + C_3 C_2 + C_3 C_1$$

SoP

③

$$C_3 C_1 \rightarrow$$

	C_4	C_2	C_0	
	\downarrow	\downarrow	\downarrow	
	x	$\cdot C_3$	$\cdot x$	$\cdot C_1$
		$\cdot x$		$\cdot x$
				$\cdot x$

$0 \ 1 \ 0 \ 1 \ 0$	$\rightarrow m_{10}$
$0 \ 1 \ 0 \ 1 \ 1$	$\rightarrow m_{11}$
$0 \ 1 \ 1 \ 1 \ 0$	$\rightarrow m_{14}$
$0 \ 1 \ 1 \ 1 \ 1$	$\rightarrow m_{15}$
$1 \ 1 \ 0 \ 1 \ 0$	$\rightarrow m_{26}$
$1 \ 1 \ 0 \ 1 \ 1$	$\rightarrow m_{27}$
$1 \ 1 \ 1 \ 1 \ 0$	$\rightarrow m_{30}$
$1 \ 1 \ 1 \ 1 \ 1$	$\rightarrow m_{31}$

$$C_3 C_2 \rightarrow$$

$$x \cdot C_3 \cdot C_2 \cdot x \cdot x$$

$m_{12}, m_{13}, m_{14}, m_{15}$
 $m_{28}, m_{29}, m_{30}, m_{31}$

$$C_4 \rightarrow C_4(C_3 + C_3') = C_4 C_3 + C_4 C_3' = \dots$$

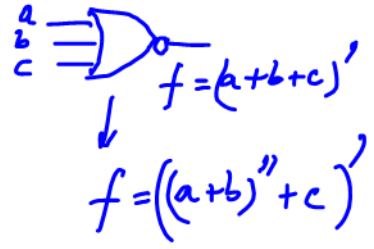
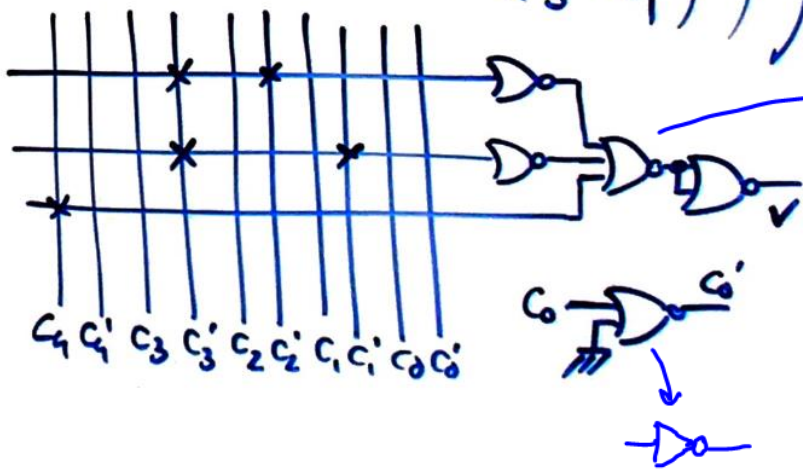
$$C_4 \cdot x \cdot x \cdot x \cdot x \Rightarrow m_{16}, m_{17}, \dots, m_{31}$$

$$V = \sum m(10, 11, 12, 13, 14, 15, 16, \dots, 31)$$

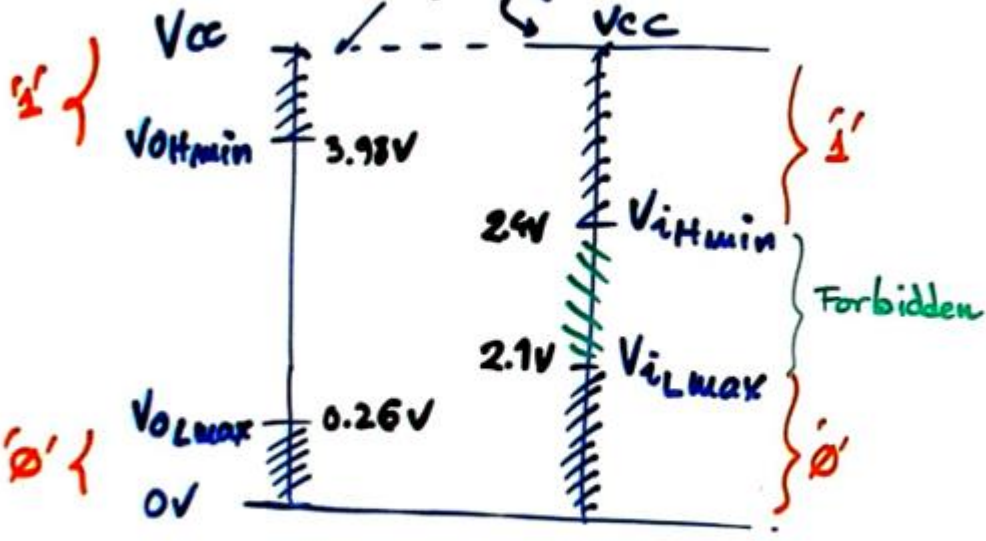
4

$$\begin{aligned}
 V &= C_4 + C_3 C_2 + C_3 C_1 \\
 &= (C_4 + (C_3 \cdot C_2)'' + (C_3 C_1)'')'' \\
 &= \left((C_4 + (C_3' + C_2')') + (C_3' + C_1')' \right)'
 \end{aligned}$$

1. Using NOR
2. NOR 3-input \rightarrow with NOR 2-inputs

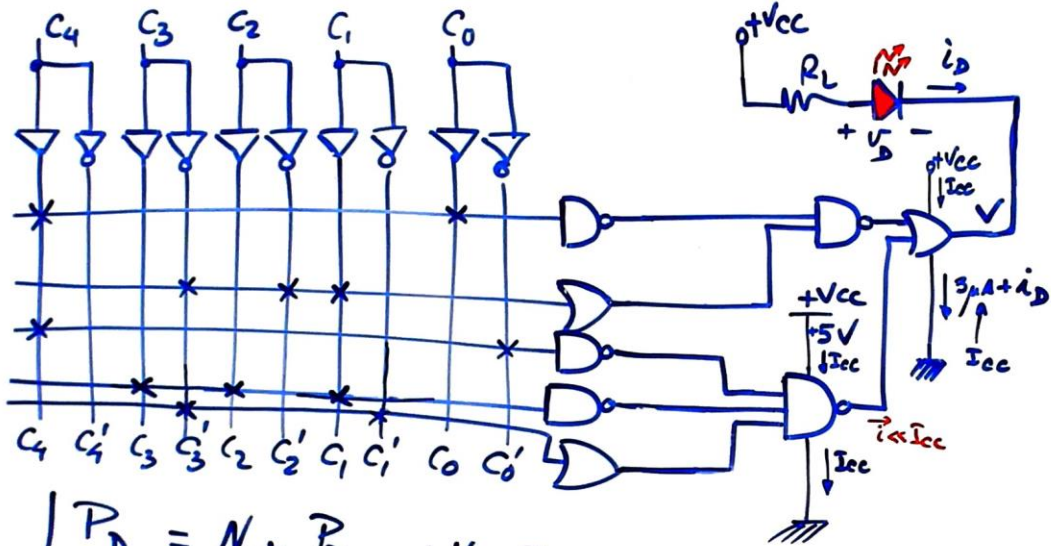


5



$$\begin{aligned}
 NMH &= V_{OHmin} - V_{iHmin} = 1.58V \\
 NML &= V_{iLmax} - V_{OLmax} = 1.84V
 \end{aligned}$$

6

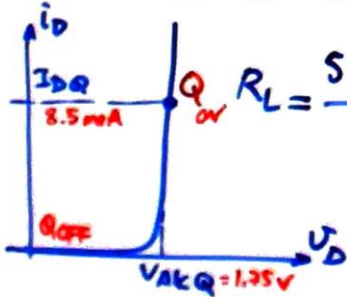


$$\begin{cases} P_{D\text{ ON}} = N_{\text{gates}} P_{D\text{ gate}} + V_{CC} I_{DQ} & \text{when ON} \\ P_{D\text{ OFF}} = N_{\text{gates}} \cdot P_{D\text{ gate}} & \text{when OFF} \end{cases}$$

$$P_{D\text{ ON}} = 18 \cdot 15 \mu\text{W} + 5\text{V} \cdot 8.5\text{mA} = 42.77\text{mW}$$

$$P_{D\text{ OFF}} = 270 \mu\text{W}$$

$$V_{CC} = R_L \cdot i_D + V_D + V_0 \rightarrow R_L = \frac{V_{CC} - V_{AKQ} - V_{OL\text{max}}}{I_{DQ}}$$



7 To complete the truth table simulation:

$$2.7\text{ns} = t_p$$



4 levels of gates

$$t_{p\text{ circuit}} = 4 \cdot t_{p\text{ gate}} = 10.8\text{ns}$$

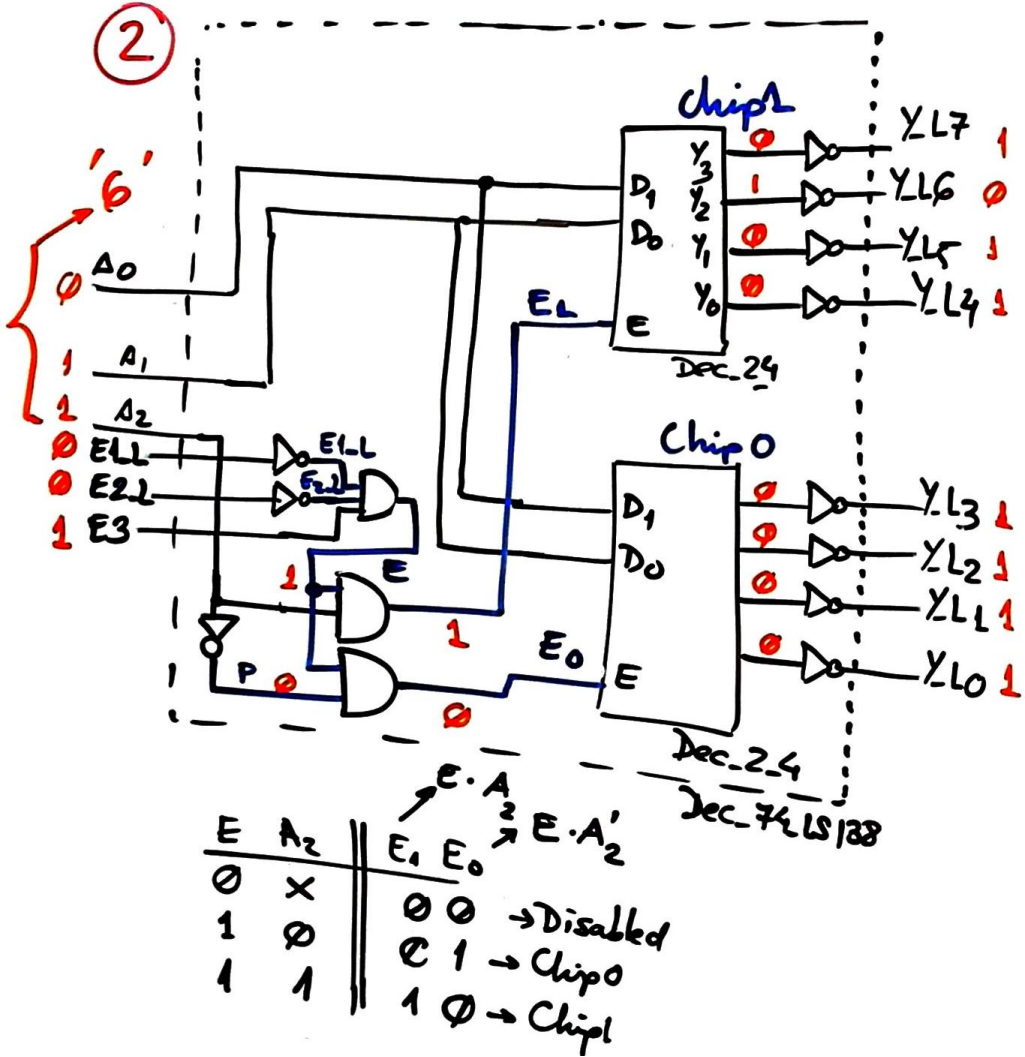
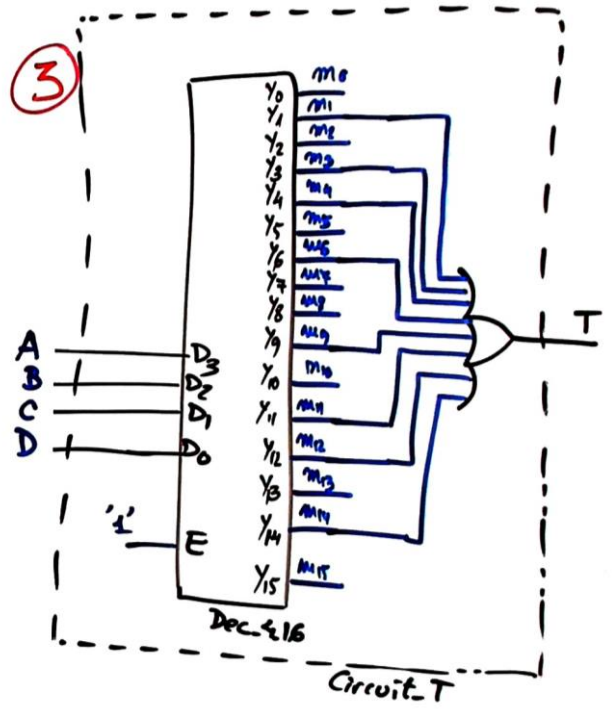
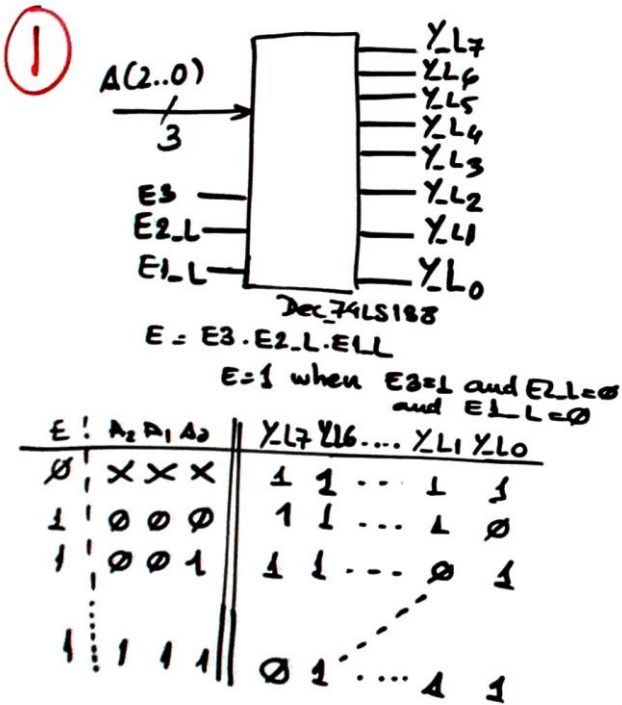
Thus, if Min.Pulse = $t_{p\text{ circuit}}$

minimum simulation time

$$t_{\text{run}} \geq 2^5 \cdot t_{p\text{ circuit}} = \underline{346\text{ns}}$$

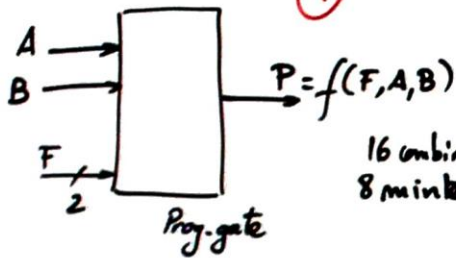
$$T = \sum m(1, 3, 4, 6, 9, 11, 12, 14)$$

Problem 2



Problem 3

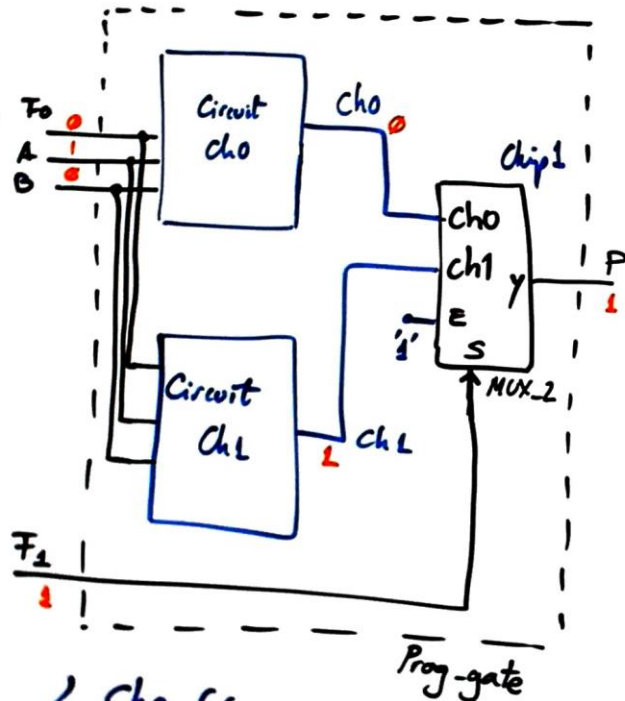
①



16 combinations
8 minterms

	F _i	F ₀	A	B	P
NOR	0	0	0	0	1
	0	0	0	1	0
	0	0	1	0	0
	0	0	1	1	0
NAND	0	1	0	0	1
	0	1	0	1	1
	0	1	1	0	1
	0	1	1	1	1
XOR	1	0	0	0	0
	1	0	0	1	0
	1	0	1	0	0
	1	0	1	1	0
NXOR	1	1	0	0	1
	1	1	0	1	0
	1	1	1	0	0
	1	1	1	1	0

②



$$\begin{cases} \text{cho} = f(F_0, A, B) = \sum m(0, 4, 5, 6) \\ \text{chl} = f(F_0, A, B) = \sum m(1, 2, 4, 7) \\ \text{gates (Buffer-NOT-AND-OR)} \\ \text{MUX-2.vhd} \\ \text{Prog.gate.vhd} \end{cases}$$

③

Assuming Circuit cho and Circuit chl and MUX-2 of 3 levels of gates



$$\begin{aligned} t_p &= 6 \cdot t_{p_{\text{gate}}} = 16.2 \text{ ns} \\ f_{\text{max}} &= 61.7 \text{ MHz} \end{aligned}$$

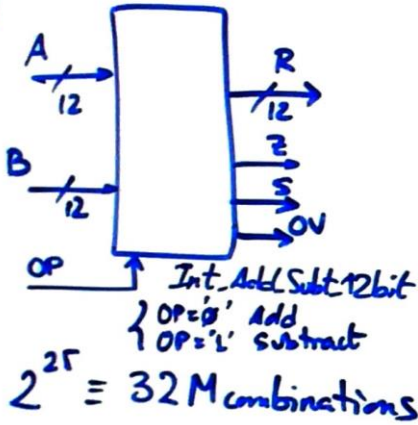
If P = f(F, A, B) is solved using 3 levels of gates

$$t_p = 3 \cdot t_{p_{\text{gate}}} = 8.1 \text{ ns}$$

$$\begin{aligned} f_{\text{max}} &= 123.5 \text{ MHz} \\ &\text{(faster than using plan C2)} \end{aligned}$$

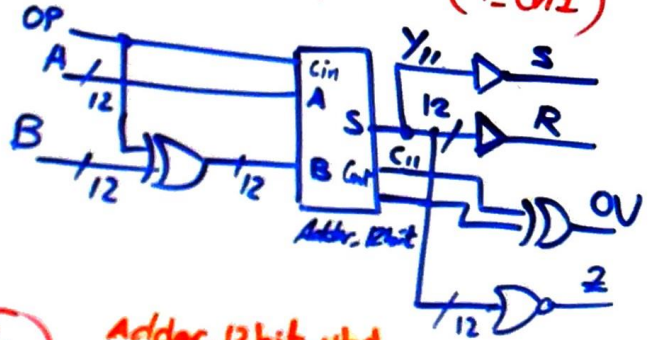
Problem 4

①



range 12 bit, integer, 2C
 $-2^{11} \leq A, B, R \leq +2^{11}-1$
 $-2048 \leq A, B, R \leq +2047$

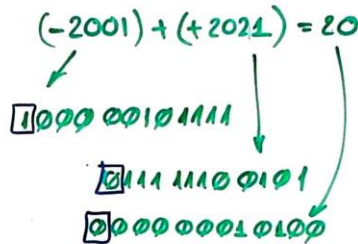
③ → Architecture plan C2 (P.Ch1)



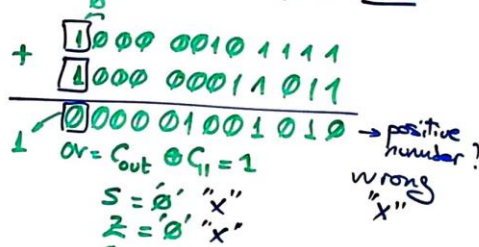
④ Adder: 12 bit. vhd
 Int. Add. Subt. 12 bit. vhd
 Adder. 1 bit. vhd

②

OP = 0' R = A + B (-2001) + (+2021) = 20
 S = 0'
 Z = 0'
 OV = 0'



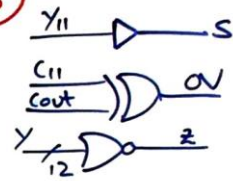
OP = 1' R = A - B (-2001) - (+2021) → OV = 1



OP = 1' R = A - B (-1474) - (+1598)
 S = 0' "x"
 Z = 0' "x"
 OV = 1
 overflow out of range

OP = 0' R = A + B (-1474) + (+1598)
 S = 0
 OV = 0 Z = 0
 +64+32+16+12 = 124

⑤



⑥

tp = 2.7 ns

If Adder: 12 bit →
 12 × Adder: 1 bit (ripple carry)
 3 levels of gates

$$t_p = (1 + 12 \times 3 + 1) t_{p, \text{gate}}$$

$$t_p = 38 \cdot t_{p, \text{gate}} = 102.6 \text{ ns}$$

⑦

9.75 Moperations/s
 ModelSim gate-level simulation

$$\text{Min. Pulse} = 102.6 \text{ ns}$$

Simulation run time to solve all the truth table

$$\text{runtime} = 2^{25} * \text{Min. Pulse} = 3.44 \text{ s}$$