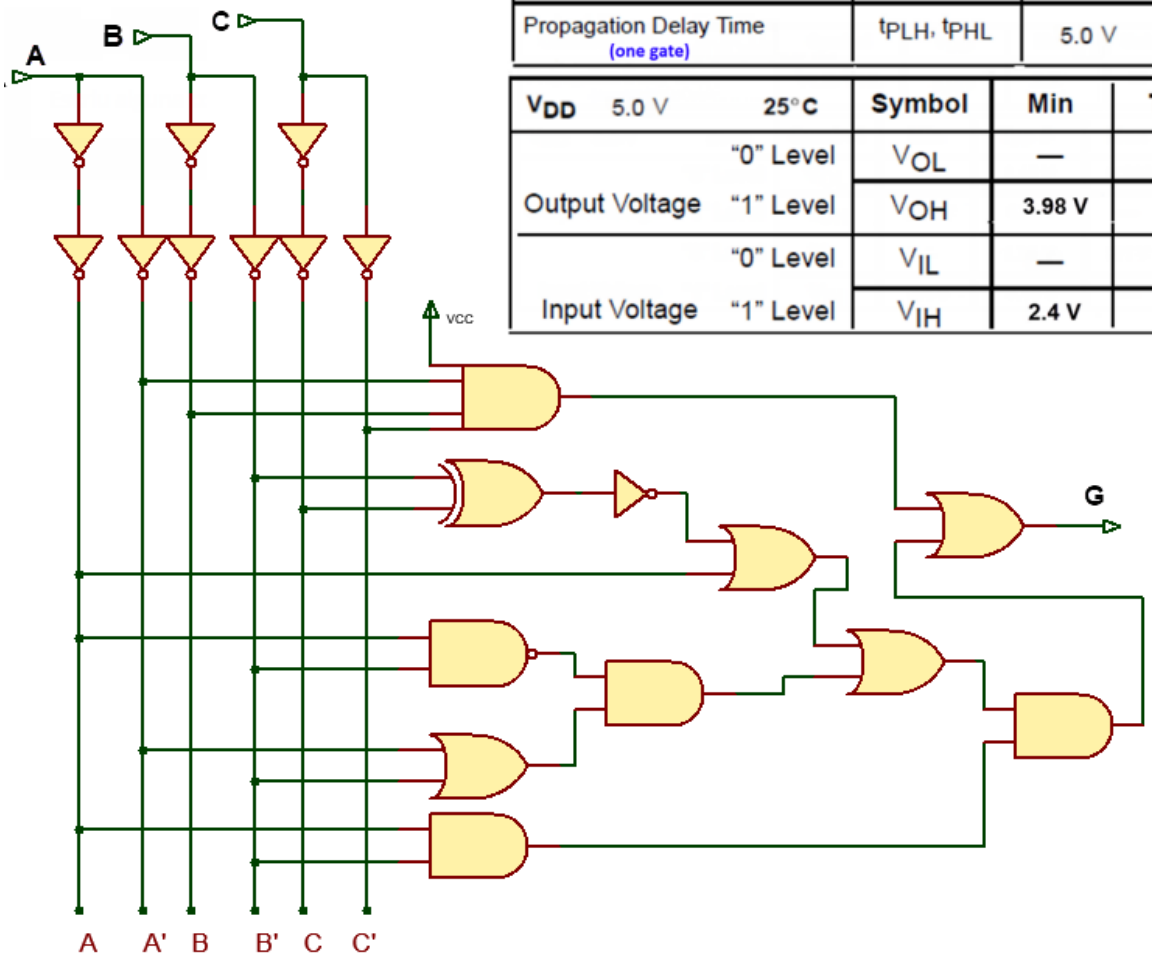
UPC. EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). Dr F. J. Robert. Grades will be available online on April 28th. Questions about the exam at office time.

Exam 1. **April 21st, 2021**

Problem 1. (4p)

Analysis

Analyse the digital circuit in Fig. 1. This means finding the circuit's truth table **G = *f*(A, B, C)**.



Characteristic	Symbol	V_{DD}	Max	Unit
Propagation Delay Time (one gate)	t_{PLH}, t_{PHL}	5.0 V	2.7	ns

V_{DD} 5.0 V 25°C		Symbol	Min	Typ #	Max
Output Voltage	"0" Level	V_{OL}	—	0.15 V	0.26 V
	"1" Level	V_{OH}	3.98 V	4.32 V	—
Input Voltage	"0" Level	V_{IL}	—	1.35 V	2.1 V
	"1" Level	V_{IH}	2.4 V	3.15 V	—

Fig. 1. Circuit to analyse. Electrical characteristics of the logic family.

a) Draw your analysis plan using a concept map.
b) Find the circuit's algebraic equation.
c) Apply Boolean algebra to simplify and obtain SoP (or PoS).
d) From SoP (or PoS), add missing variables to deduce the circuit's truth table.
e) Calculate the timing diagram when the input signals are represented as waveforms in Fig. 2.
f) Represent logic values, voltages and noise margins for this logic family.
g) If a single gate dissipates 35 µW, calculate circuit power consumption when G is driving an active-high LED with I_{DQ} = 5.5 mA and V_{AKQ} = 1.85 V. Calculate the LED's limiting resistor.
h) How fast is the circuit performing the truth table?

Design

i) Design the circuit using maxterms.
j) Design the circuit using only NOR of 2 inputs.
k) Design the circuit using the method of multiplexers and a MUX_2.
l) Design the circuit using the method of decoders.

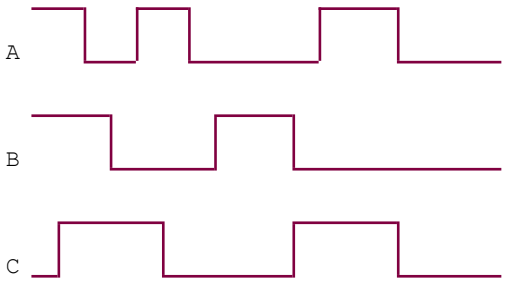
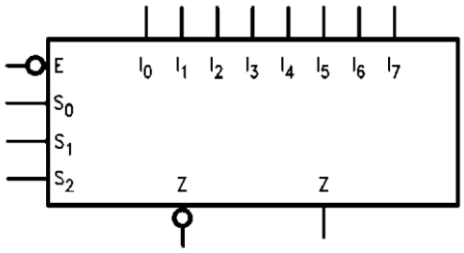


Fig. 2.

Problem 2. (2p)

Fig. 3 is the standard CD74AC151 chip, a commercial 8-channel digital multiplexer (*MUX_8*).

a) Rename inputs and outputs using our CSD style and draw its symbol and truth table.
b) Design it using our elemental block *MUX_2* following plan C2 based on a hierarchy of components.
c) How many VHDL files will require your circuit?



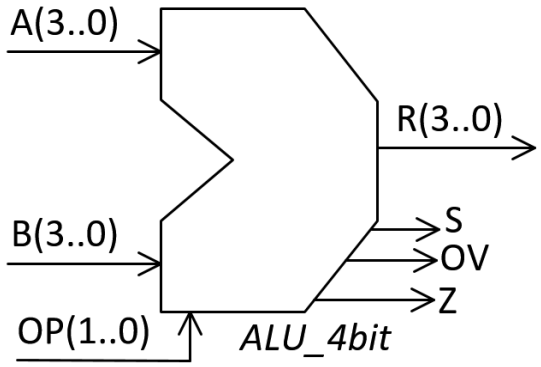
Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

Pin Names	Description
I_0–I_7	Data Inputs
S_0–S_2	Select Inputs
$\overline{E}$	Enable Input
Z	Data Output
$\overline{Z}$	Inverted Data Output

Fig. 3. CD74AC151 standard chip.

Problem 3. (4p)

We have in mind inventing the circuit in Fig. 4 for performing simple 4-bit arithmetic and logic operations.



OP	Function	
00	A – B	Arithmetic (4-bit signed integer in two's complement)
01	A + B	Arithmetic (4-bit signed integer in two's complement)
10	A ⊕ B	Logic XOR
11	(A · B)'	Logic NAND

Flags: **S**: sign bit; **OV**: overflow situation; **Z**: zero result.

Fig. 4. Symbol and operations performed by the arithmetic and logic unit (*ALU_4bit*).

a) How long is the circuit's truth table? How many maxterms does Z flag contain?
b) Deduce some examples of the circuit's truth table solving the four operations for the following data (12 stimulus). Express inputs and outputs in the right radix and indicate *don't care* ('x') results when necessary.

```
A = "0101"      B = "1010"
A = "1111"      B = "1001"
A = "1000"      B = "1000"
```

OP	A	B	R	S	OV	Z

c) Propose an internal architecture for this *ALU_4bit* circuit based on plan C2. Use as component a 4-channel quadruple multiplexer (Quad_MUX_4) and other blocks and logic gates if necessary. Determine how many VHDL file contain your architecture.
d) Design flag indicators **S**, **OV** and **Z** using logic gates.
e) Invent the XOR block using only NAND.