Problem 1

a) $F = g(C,B,A) = \underline{\underline{\left[B(A'+C) \cdot (A+B'C')' \right]'}}$

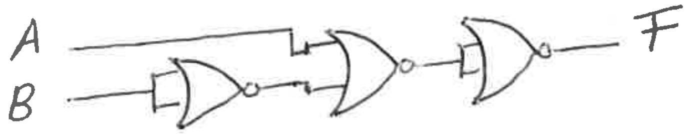
b) $F = (B(A'+C))' + (A+B'C') =$

$= B' + (A'+C)' + A + B'C' =$

$= B' + AC' + A + B'C' = A(1+C') + B'(1+C') =$

$= \underline{\underline{A + B'}}$

c) $F = A + B' = (A+B')''$



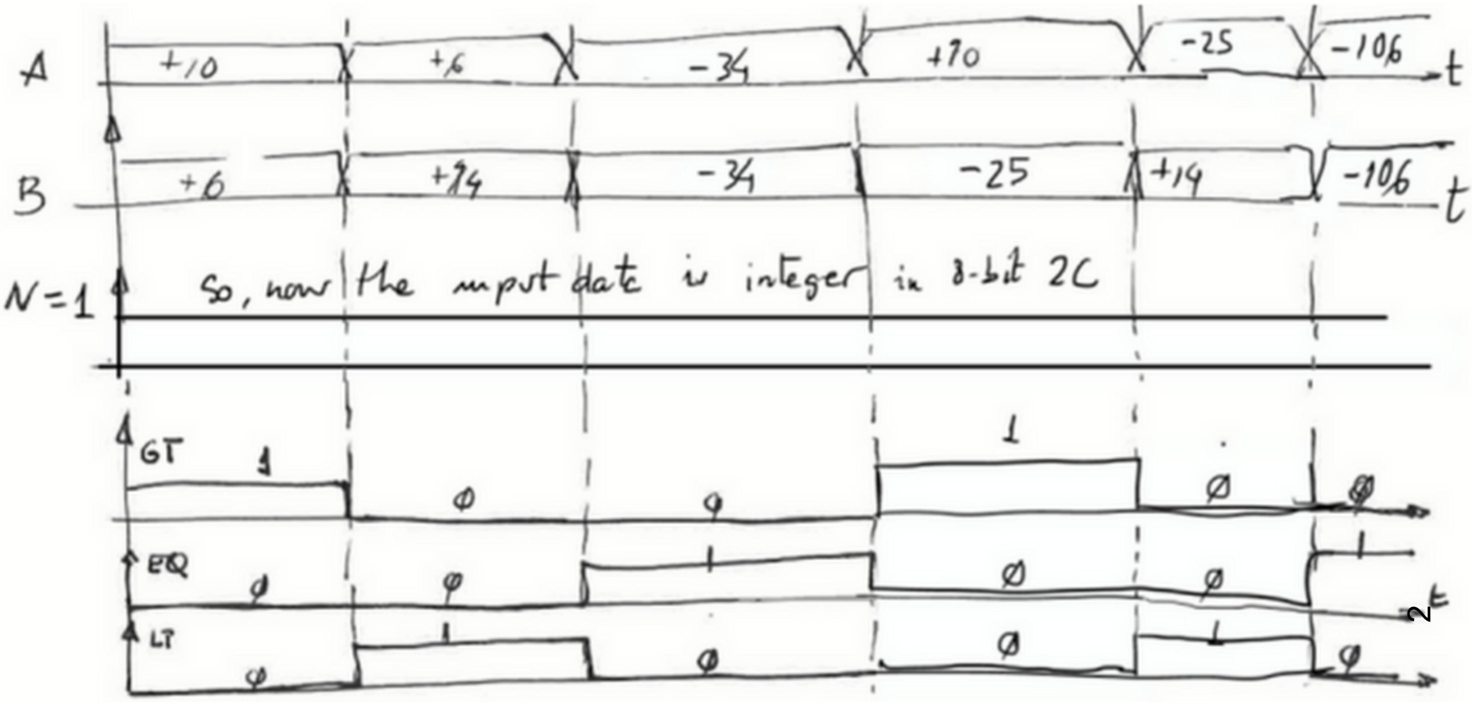
d)

C	B	A	$F = A+B'$
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

$F = \prod_3 (2,6) = \underline{\underline{(C+B'+A)(C'+B'+A)}}$

Problem 2 (Similar problem from 1819Q2)

a)



A	B	N	GT	EQ	LT
10	6	0	1	0	0
6	14	0	0	0	1
222	222	0	0	1	0
10	231	0	0	0	1
231	14	0	1	0	0
150	150	0	0	1	0
b) +10	+6	1	1	0	0
+6	+14	1	0	0	1
−34	−34	1	0	1	0
+10	−25	1	1	0	0
−25	+14	1	0	0	1
−106	−106	1	0	1	0

etc.

Radix-2 unsigned decimal

$10 \rightarrow (00001010)_2$

$14 \rightarrow (00001110)_2$

$6 \rightarrow (00000110)_2$

$222 \rightarrow (1101\ 1110)_2$

$231 \rightarrow (11100111)_2$

$150 \rightarrow (10010110)_2$

Integer → signed decimal

$+10 \leftrightarrow \boxed{0}0001010$

$+14 \leftrightarrow \boxed{0}0001110$

$+6 \leftrightarrow \boxed{0}0000110$

$-34 \leftarrow \boxed{1}1011110$

$-25 \leftarrow \boxed{1}1100111$

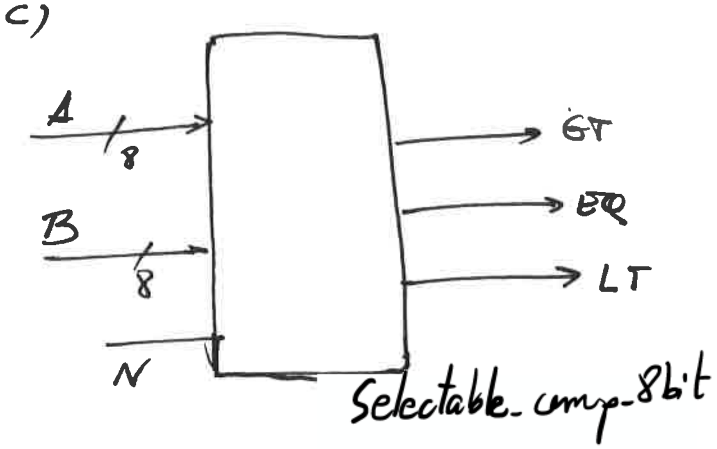
$-106 \leftarrow \boxed{1}0010110$

$\boxed{0}1101001$
$+1$

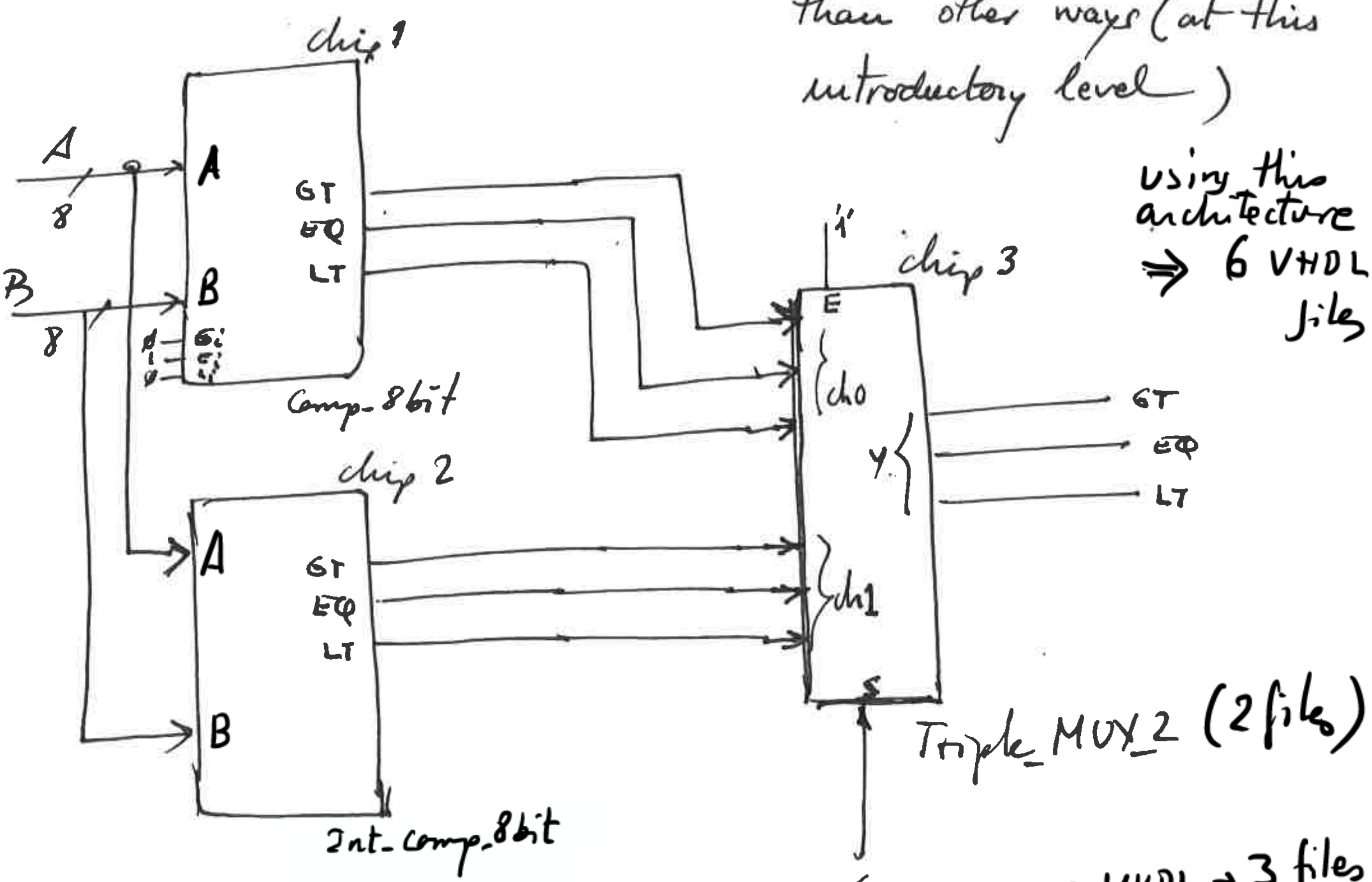
$\underbrace{\boxed{0}1101010}_{+106}$ → -106

→ The idea is that with a $n = 8$ it is only possible to represent signed integers in 2C from $-128 \le A, B, \le +127$ and **radix-2 numbers** from $0 \le A, B \le 255$

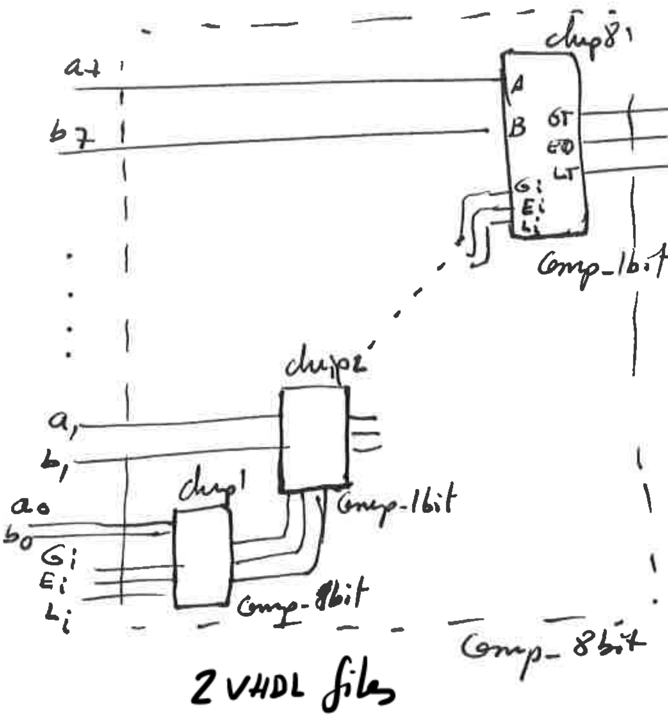
c)



This circuit may be designed using the plan C2 because it is too large and basing it on smaller chips is simpler than other ways (at this introductory level)

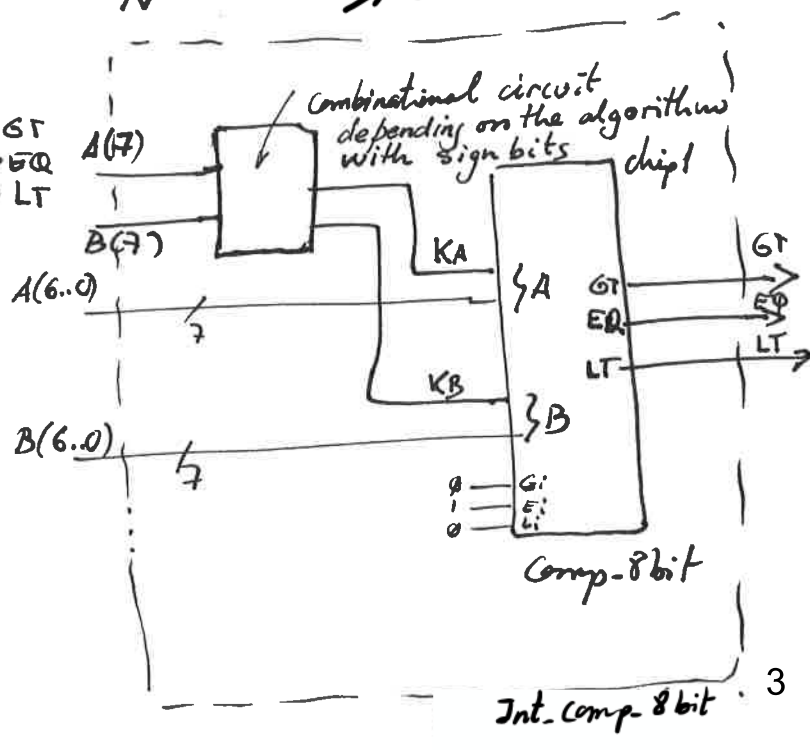


using this architecture ⇒ 6 VHDL files

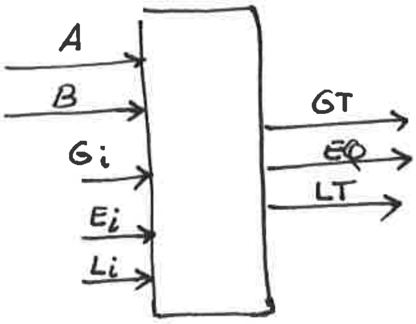


2 VHDL files

→ VHDL → 3 files



d)



Comp_1bit

Plan A	Plan B	Plan C2
gate equations	truth table or algorithm	using components

Plan A (gate equations):

- → canonical (maxterms / minterms)
- → SoP / PoS (using 'minilog')
- → any kind of equation

A	B	Gi	Ei	Li	GT	EQ	LT
1	0	-	-	-	1	0	0
0	1	-	-	-	0	0	1
1	1	1	0	0	1	0	0
1	1	0	1	0	0	1	0
1	1	0	0	1	0	0	1
0	0	1	0	0	1	0	0
0	0	0	1	0	0	1	0
0	0	0	0	1	0	0	1

Incomplete functions

other combinations (xxx)

2^5 → 32 different combinations

(Some of them don't care, like 00110
00101
00011
⋮)

Thus, if $\boxed{\text{Plan A}}$ has to be used, and canonical equations based on $\boxed{\text{maxterms}}$, we have to find how many maxterms GT, EQ and LT have.

A	B	Gi	Ei	Li	GT	
0	1	x	x	x	0	→ $M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}$
1	1	0	1	0	0	→ M_{26}
1	1	0	0	1	0	→ M_{25}
0	0	0	1	0	0	→ M_2
0	0	0	0	1	0	→ M_1

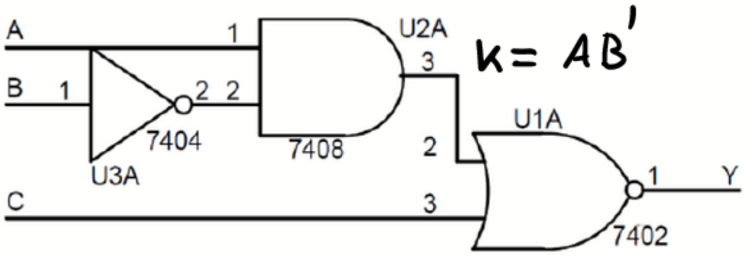
⇒ 12 maxterms

(assuming that other terms don't care are considered '1', like
00110
00101
00111
⋮)

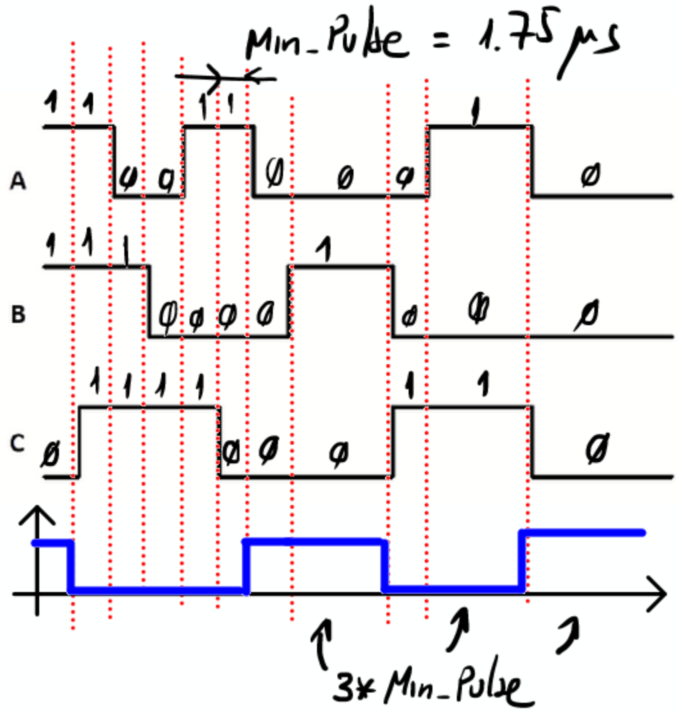
EQ → 20 maxterms

LT → 12 maxterms

Problem 3



$K = AB'$



$$K = A \cdot B'$$

$$Y = (K + C)' = (AB' + C)'$$

$$(AB')' \cdot C' = (A' + B) \cdot C' = A'C' + BC'$$

$$Y = A'BC' + A'B'C' + ABC' + A'BC'$$

$$Y = m_{010} + m_{000} + m_{110} + m_{010}$$

$$Y = f(A,B,C) = \sum_3 m(0,2,6)$$

from which the timing diagram can be represented immediately

For example $y(111) = (1 \cdot 1' + 1)' = (0 + 1)' = 0$

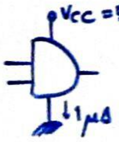
$$Y(110) = (1 \cdot 1' + 0)' = (0 + 0)' = 1$$

$$Y(011) = (0 \cdot 1' + 1)' = 1' = 0$$

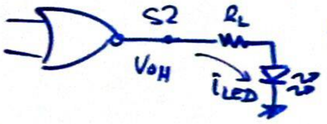
Simulation time $\simeq$ 8 · Min_Pulse + 9 · Min_Pulse $\sim$ 30 μs

Problem 4

a) Power consumption $\underbrace{5V \times 1\mu A}_{5\mu W} \times 64 = 320\,\mu W$



64 gates



$V_{OH} = R_L \cdot I_{LED} + V_{AK}$

$R_L = \dfrac{V_{OH\,min} - V_{AK}}{I_{LED}}$

$= \dfrac{4.95V - 1.65V}{7mA}$

$R_L = 471.4\Omega \simeq \underline{470\Omega}$

b) Number of gate levels means the lenght of the circuit from input to output, determining the circuit's propagation delay

Aprox:

$S_1 \to 6$

$S_2 \to 10$

$S_3 \to 11$

$\boxed{S_4 \to 14}$ → For example from B3 to S4

Cout → 11

c) From A or B to S ⇒ $t_p = 2100\,ns$

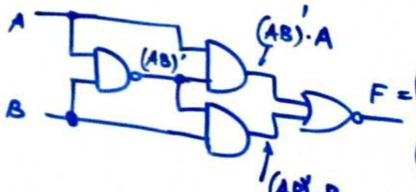
If we consider 14 levels of gates

$t_p = \dfrac{2100}{14} ns = 150ns$

This circuit can perform a maximum number of operations ≤ $\dfrac{1}{2100ns} = 476\,190$ operations/s

d) Gate-level simulation allows the simulation of the flattened technology schematic synthesised into a target chip of a given vendor.

e)



$F = \left((AB)' \cdot A + (AB)' \cdot B\right)'$

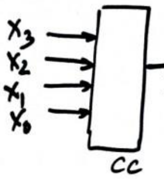
$\left(((A \cdot B)'(A+B)\right)'$

$\left(\underbrace{(A'+B')(A+B)}_{G = M_{11} \cdot M_{00}}\right)' = G'$

A B	G	F = G'
0 0	0	1
0 1	1	0
1 0	1	0
1 1	0	1

$F = (A \oplus B)'$

Problem 5

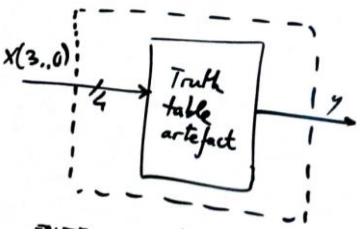


$y = \prod_4 M(0,1,3,6,8,9,10,13,14)$

$y = f(x_3, x_2, x_1, x_0)$

a) Plan B means capturing the truth table directly in VHDL

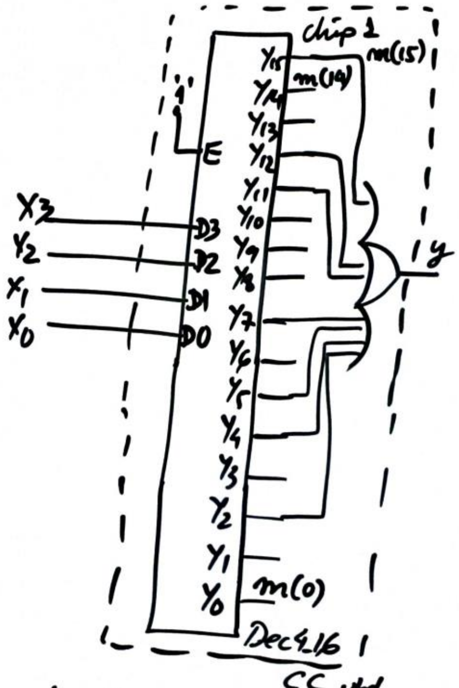
→ In this case there is no need for a signal because the input is already expressed as the vector X(3..0)




```
ENTITY CC is
   port (
   X : IN std_logic_vector(3 downto 0);
   Y : OUT std_logic
   );
end CC;
```

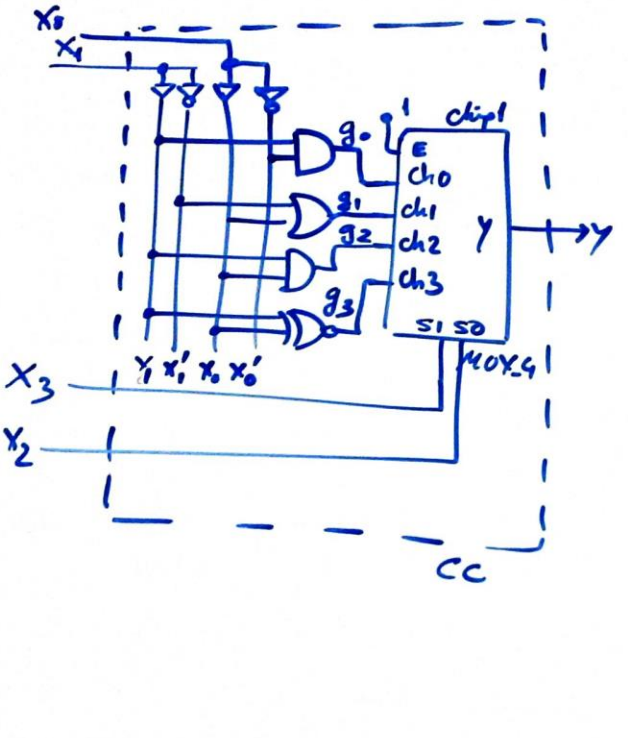
```
Architecture plan_B of CC is
begin
  process (X)
    begin CASE X IS:
    when "0000" =>
            Y <= '0';
    when "0001" => Y <= '0';
    when "0010" => Y <= '1';
         ⋮
    when "1110" =>
            Y <= '0';
    when others => Y <= '1';
    end CASE;
   end process;
 end plan_B;
```

b) Method of decoders (MoD)



$y = f(x) = \sum_4 m(2,4,5,7,11,12,15)$

c) Method of multiplexers (MoM) using a MUX-4

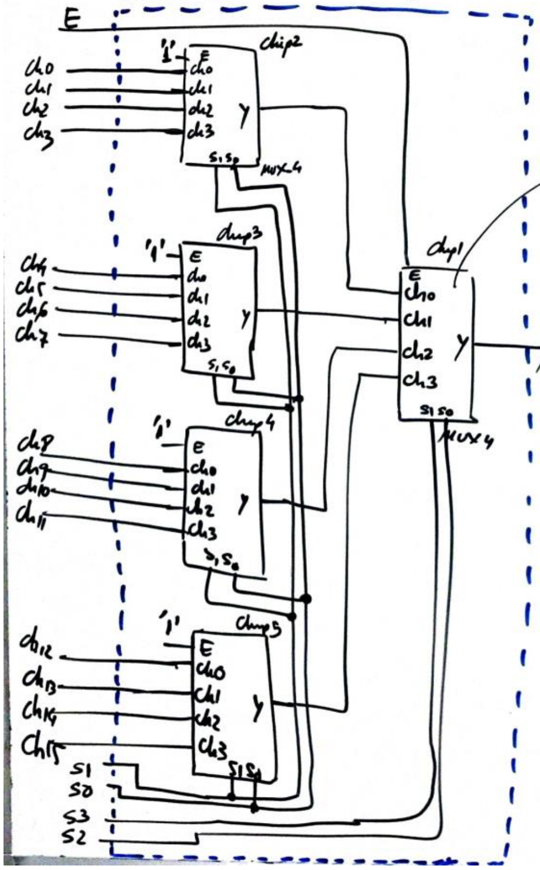


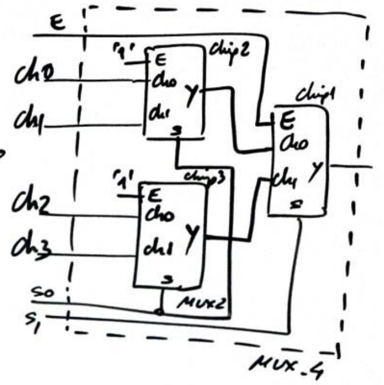
* Representation of the CC truth table subdivided in 4 channels

	X3	X2	X1	X0	Y	
Ch0	0	0	0	0	0	$g_0 = x_1 \cdot x_0'$
	0	0	0	1	0	
	0	0	1	0	1	
	0	0	1	1	0	
Ch1	0	1	0	0	1	$g_1 = x_1' + x_0$
	0	1	0	1	1	
	0	1	1	0	0	
	0	1	1	1	1	
Ch2	1	0	0	0	0	$g_2 = x_1 \cdot x_0$
	1	0	0	1	0	
	1	0	1	0	0	
	1	0	1	1	1	
Ch3	1	1	0	0	1	$g_3 = (x_1 \oplus x_0)' = x_1' \cdot x_0' + x_1 \cdot x_0$
	1	1	0	1	0	
	1	1	1	0	0	
	1	1	1	1	1	

S1 S0

d) Mux_16 solved using plan C2 (hierarchical design)





e)

$$y = f(\underline{X}) = \prod_4 M(0,1,3,6,8,9,10,13,14)$$

Solve the function using the MoM

and a MUX_16

Let's connect the truth table to the corresponding channel