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Questions about the exam: Lecturer's office hours. Grades will be available on April 16.

Exam 1 **April 9, 2018**

Problem 1. (5p)

1. Draw the symbol and an example of timing diagram for the combinational circuit with the truth table represented in Fig. 1. Use a *Min_Pulse* time constant of 1.5 µs and explain how long it takes to run a test bench simulation of the circuit. Indicate a possible application of this digital circuit. (1p)

B_1	B_0	A_1	A_0	R_3	R_2	R_1	R_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

```
===========
BBAA   RRRR
1010   3210
===========
1111 | 1...
1-10 | .1..
101- | .1..
-110 | ..1.
1-01 | ..1.
10-1 | ..1.
011- | ..1.
-1-1 | ...1
```

Fig. 1
The truth table of a combinational circuit and its SoP minimisation result in Minilog table output format.

2. Express $R_2 = g(B_1,B_0,A_1,A_0)$ as a sum of minterms and $R_1 = f(B_1,B_0,A_1,A_0)$ as a product of maxterms. (0.5p)

3. Draw the hierarchical schematic of a digital circuit that implements the outputs of the digital circuit using a DEC_4_16 and explain how many VHDL files the project contains. (1p)

4. Draw the hierarchical schematic of a digital circuit that implements the output R_1 of the digital circuit using the method of multiplexers and a MUX_4. Explain how many VHDL files the project contains. (1p)

5. Generate a flat circuit using the SoP results from the Minilog table output format in Fig. 1. Write the VHDL statements corresponding to this structural architecture. (0.5p)

6. Implement the output R_3 using only 2-input NOR logic gates. (0.5p)

7. The circuit in section 5 above will be implemented using a classic technology ALS with the characteristics shown in Fig. 2. Deduce and explain the maximum speed of computing and the power consumption when powered at 5 V. Assume that the current consumption of a single logic gate is $I_{CC} = (I_{CCH}+I_{CCL})/2$. (0.5p)

PARAMETER	SN74ALS04B MIN	SN74ALS04B TYP	SN74ALS04B MAX	UNIT
V_{IK}			−1.2	V
V_{OH}	V_{CC} −2			V
V_{OL}		0.25	0.4	V
		0.35	0.5	
I_I			0.1	mA
I_{IH}			20	µA
I_{IL}			−0.1	mA
I_O#	−30		−112	mA
I_{CCH}		0.65	1.1	mA
I_{CCL}		2.9	4.2	mA

		SN74ALS04B MIN	SN74ALS04B NOM	SN74ALS04B MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

	MIN	MAX	
t_{PLH}	3	11	ns
t_{PHL}	2	8	

Fig. 2
Technology characteristic for the logic family ALS-TTL

Problem 2. (5p)

1. Draw the symbol and the hiearchical internal schematics of a 7-bit two's complement adder/subtractor (*Adder_Subtractor_7bit*). How many VHDL files the project will include? Name all the VHDL source files and explain their function. (1p)

2. Determine the range of the operants **A**, **B** and the result **R**. Explain how the overflow (**OV**) flag works and how its circuit and truth table can be infered.

(0.5p)

3. Perform the following operations in binary using the two's complement (2C) **7-bit** adder/subtractor from previous section 1). Check the result and deduce the **Z** and **OV** flags. (1p)

a) $(+39)_{10}$ **+** $(1001010)_{2C}$

b) $(0010110)_{2C}$ **−** $(-55)_{10}$

c) $(+18)_{10}$ **+** $(1101110)_{2C}$

d) $(-31)_{10}$ **−** $(0010110)_{2C}$

4. Represent the previous operations in a timing diagram and translate it (only the stimulus section) to a VHDL test bench using a constant *Min_Pulse* = 10.5 µs. Furthermore, calculate how long it takes to run a test bench for simulating not only the four previous operations, but all the possible input combinations.

(0.5p)

5. Determine the maximum speed of operation of the 7-bit 2C adder/subtractor if synthesised in an Altera MAX7128S CPLD device. The propagation delay of a logic gate in this technology is 2 ns. Justify your calculations.

(1p)

6. Deduce the logic function and the corresponding circuit to add the new feature of equality (**EQ**) detection. This is a flag or indicator that goes high when the operands **A** = **B**. (1p)