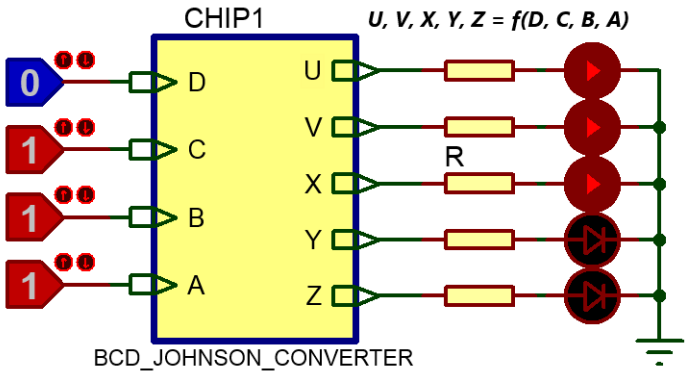
BACHELOR DEGREE IN TELECOMMUNICATIONS, Digital Circuits and Systems (CSD), March 30, 2017. Grades will be available on April 7. Questions about the exam: Instructors' office time. **It is mandatory to explain all the steps that you follow to solve each exercise in order to get grades. A student interview about the submitted work can also be requested.**

Individual Test 1 - second chance

The entity represented in Fig. 1 is a code converter from BCD to Johnson ring. Only 10 of the 16 combinations are possible, thus the other terms are don't care and you have to complete the table as you like using '0' or '1'. Rewrite the truth table in Fig. 1 and solve the questions below.



D	C	B	A	U	V	X	Y	Z
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	0	1	1	0	0	1	1	1
0	1	0	0	0	1	1	1	1
0	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	0
0	1	1	1	1	1	1	0	0
1	0	0	0	1	1	0	0	0
1	0	0	1	1	0	0	0	0
1	0	1	-	-	-	-	-	-
1	1	-	-	-	-	-	-	-

Fig. 1 The circuit for a BCD to Johnson ring code translator and its truth table.

1. Describe the algebraic expression of **V** as a product of maxterms and **U** as a sum of minterms.
2. From the table in Fig. 2, express **Z** as a sum of products (SoP), and draw the logic circuit using only NOR.
3. Build the circuit for the **Y** using the method of multiplexers and a MUX_8.
4. Build the complete circuit using the method of decoders.
5. Build the circuit using VHDL and a behavioural description of the truth table.
6. In Fig. 1, calculate the value of R for V_{CC} = 5 V, technology LSTTL, and the LED current must be set to 2.5 mA.

```
============
DCBA   UVXYZ
============
00-1  |  ....1
1--0  |  .1...
--11  |  ..1..
-01-  |  ...11
1---  |  1....
-1-1  |  11...
-110  |  1111.
-10-  |  .1111
```

a) Addition: (+108) + (-43)

b) Subtraction: (-43) - (+90)

c) Subtraction: (-90) - (-33)

d) Addition: (-121) + (+121)

Fig. 2 Output table format from Minilog.exe in SoP. *Fig. 3 Add and subtract examples in 8-bit 2C convention.*

7. Solve the arithmetic operations in Fig. 3 using 8-bit 2C (two's complement) number representation and the circuit proposed in the CSD project P4. Indicate when there is an overflow situation (OV flag). Which is the valid range of the operands and result?
8. If one gate of the circuit has a propagation delay of 3.3 ns, calculate approximately the maximus number of operations per second.