

DM74LS47

BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

The DM74LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 μ A. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions.

Features

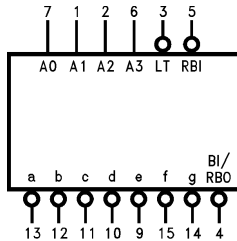
- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

Ordering Code:

Order Number	Package Number	Package Description
DM74LS47M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS47N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

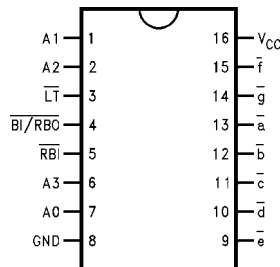
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram



Pin Descriptions

Pin Names	Description
A0-A3	BCD Inputs
RBI	Ripple Blanking Input (Active LOW)
LT	Lamp Test Input (Active LOW)
BI/RBO	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
a-g	Segment Outputs (Active LOW) (Note 1)

Note 1: OC—Open Collector

Truth Table															
Decimal or Function	Inputs							Outputs							Note
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	A3	A2	A1	A0	$\overline{\text{BI/RBO}}$	$\overline{\text{a}}$	$\overline{\text{b}}$	$\overline{\text{c}}$	$\overline{\text{d}}$	$\overline{\text{e}}$	$\overline{\text{f}}$	$\overline{\text{g}}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 2)
1	H	X	L	L	L	H	H	H	L	L	L	H	H	H	(Note 2)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{\text{BI}}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 3)
$\overline{\text{RBI}}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 4)
$\overline{\text{LT}}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 5)

Note 2: $\overline{\text{BI/RBO}}$ is wire-AND logic serving as blanking input ($\overline{\text{BI}}$) and/or ripple-blanking output ($\overline{\text{RBO}}$). The blanking out ($\overline{\text{BI}}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{\text{RBI}}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 3: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

Note 4: When ripple-blanking input ($\overline{\text{RBI}}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{\text{RBO}}$) goes to a LOW level (response condition).

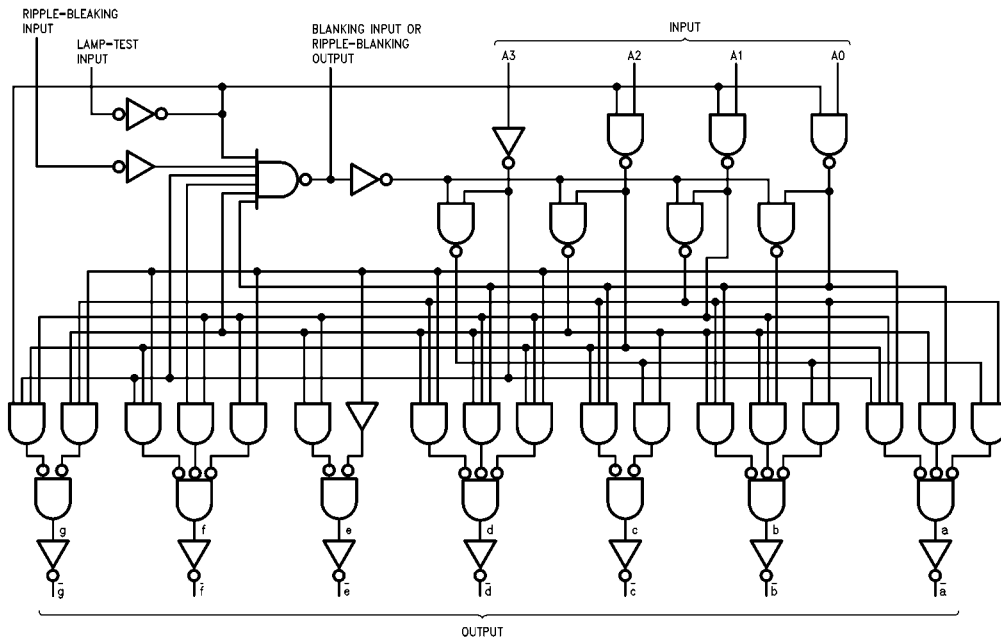
Note 5: When the blanking input/ripple-blanking output ($\overline{\text{BI/RBO}}$) is OPEN or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

Functional Description

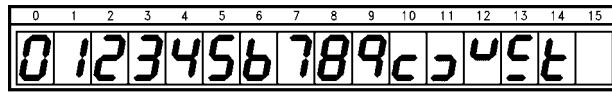
The DM74LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{\text{RBI}}$ blanks the display and causes a multi-digit display. For example, by grounding the $\overline{\text{RBI}}$ of the highest order decoder and connecting its $\overline{\text{BI/RBO}}$ to $\overline{\text{RBI}}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{\text{RBI}}$ of the lowest order decoder and connecting its $\overline{\text{BI/RBO}}$ to $\overline{\text{RBI}}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving $\overline{\text{RBI}}$ of a

intermediate decoder from an OR gate whose inputs are $\overline{\text{BI/RBO}}$ of the next highest and lowest order decoders. $\overline{\text{BI/RBO}}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{\text{RBO}}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{\text{BI/RBO}}$ can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to $\overline{\text{BI/RBO}}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{\text{LT}}$ turns on all segment outputs, provided that $\overline{\text{BI/RBO}}$ is not forced LOW.

Logic Diagram



Numerical Designations—Resultant Displays



Absolute Maximum Ratings (Note 6)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 6: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current ā - ḡ @ 15V = V _{OH} (Note 7)			-250	μA
I _{OH}	HIGH Level Output Current Bī /RBO			-50	μA
I _{OL}	LOW Level Output Current			24	mA
T _A	Free Air Operating Temperature	0		70	°C

Note 7: OFF-State at ā-ḡ.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 8)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max, Bī /RBO	2.7	3.4		V
I _{OFF}	Output HIGH Current Segment Outputs	V _{CC} = 5.5V, V _O = 15V ā - ḡ			250	μA
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min, ā - ḡ		0.35	0.5	V
		I _{OL} = 3.2 mA, Bī /RBO			0.5	
		I _{OL} = 12 mA, ā - ḡ		0.25	0.4	
		I _{OL} = 1.6 mA, Bī /RBO			0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V V _{CC} = Max, V _I = 10V			100	μA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.4	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 9), I _{OS} at Bī /RBO	-0.3		-2.0	mA
I _{CC}	Supply Current	V _{CC} = Max			13	mA

Note 8: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

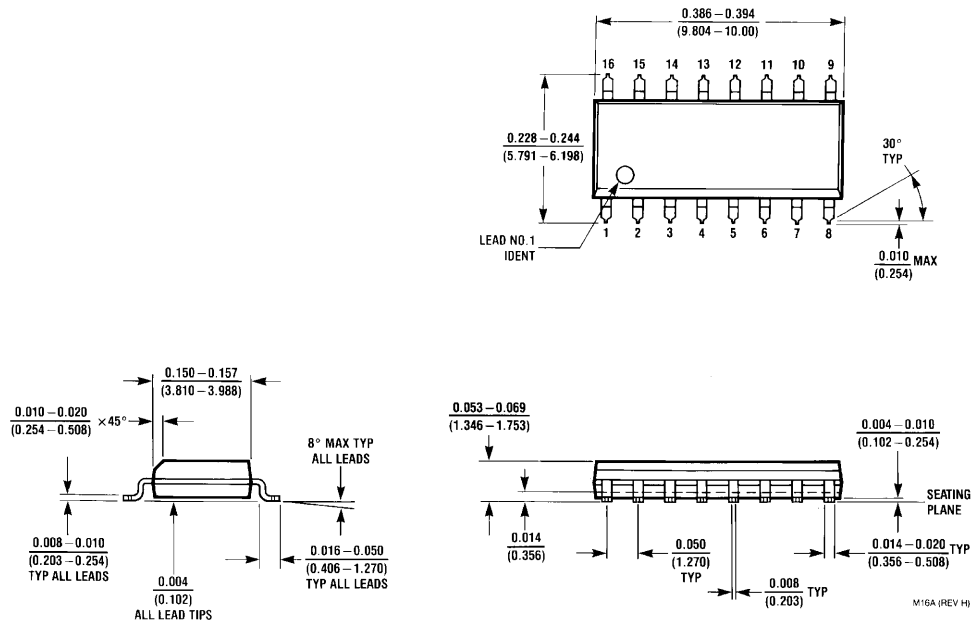
Switching Characteristics

at V_{CC} = +5.0V, T_A = +25°C

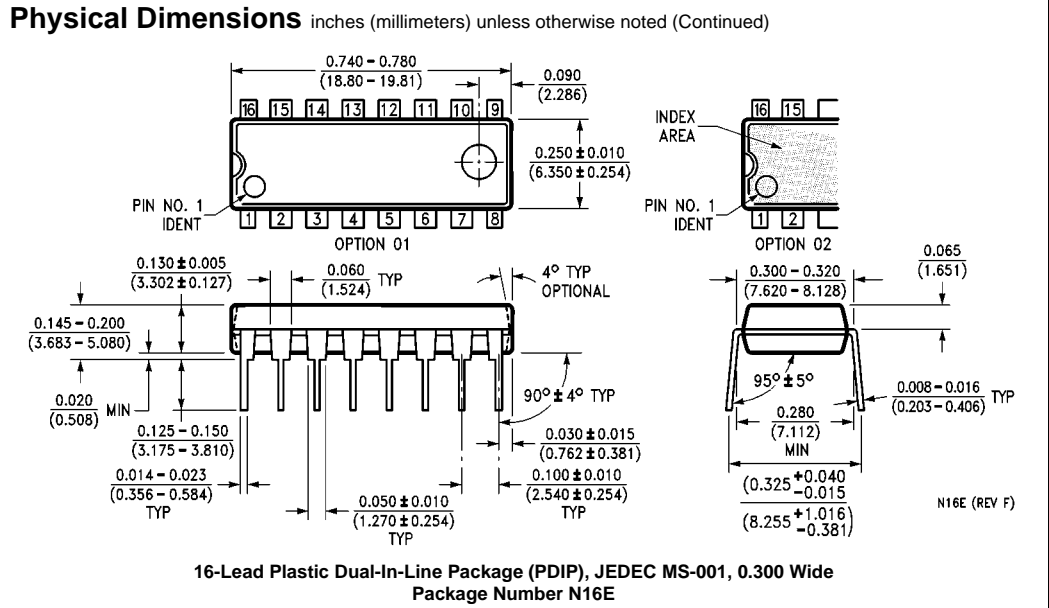
Symbol	Parameter	Conditions	R _L = 665Ω C _L = 15 pF		Units
			Min	Max	
			t _{PLH}	Propagation Delay An to ā - ḡ	
t _{PHL}			100		
t _{PLH}	Propagation Delay RBI to ā - ḡ (Note 10)		100	ns	
t _{PHL}			100		

Note 10: L_T = HIGH, A0-A3 = LOW

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com