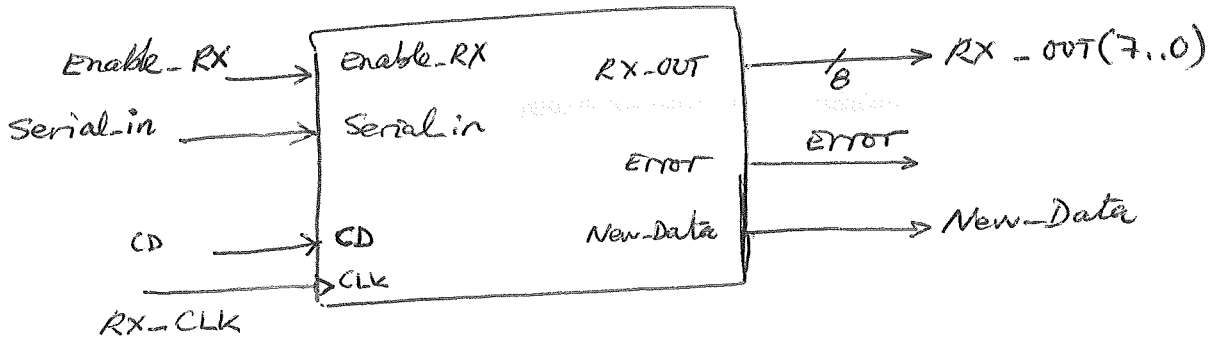
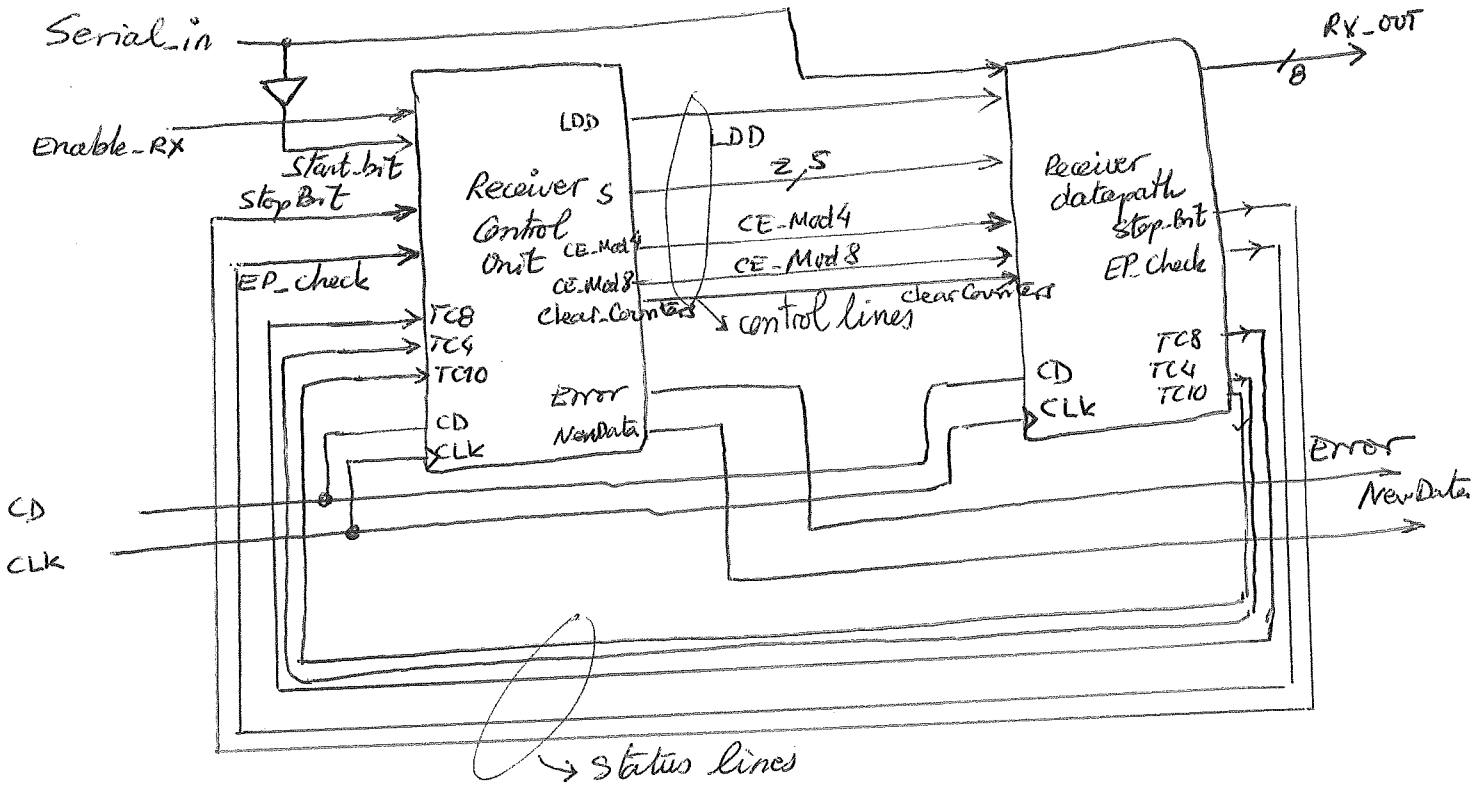
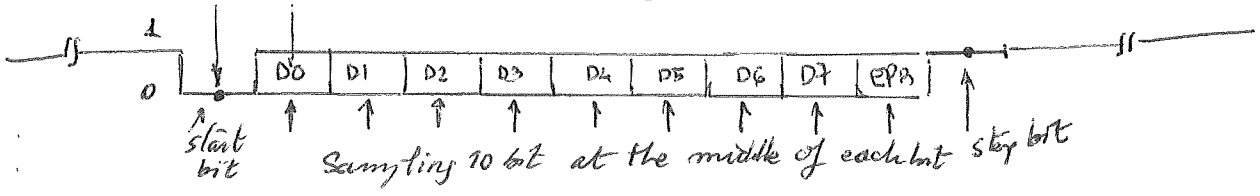
Receiver unit

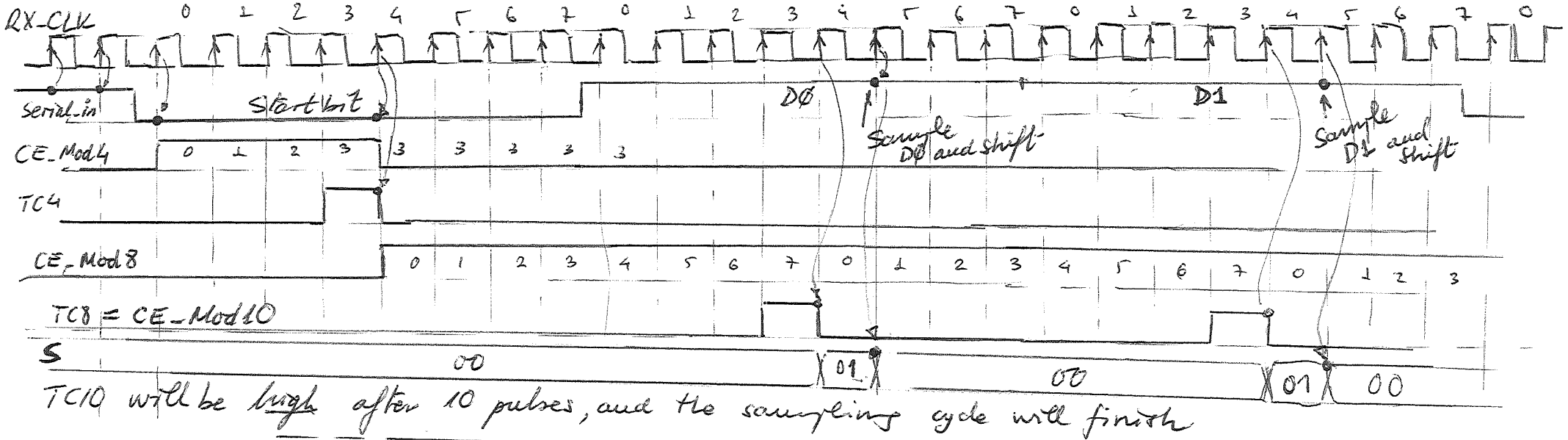




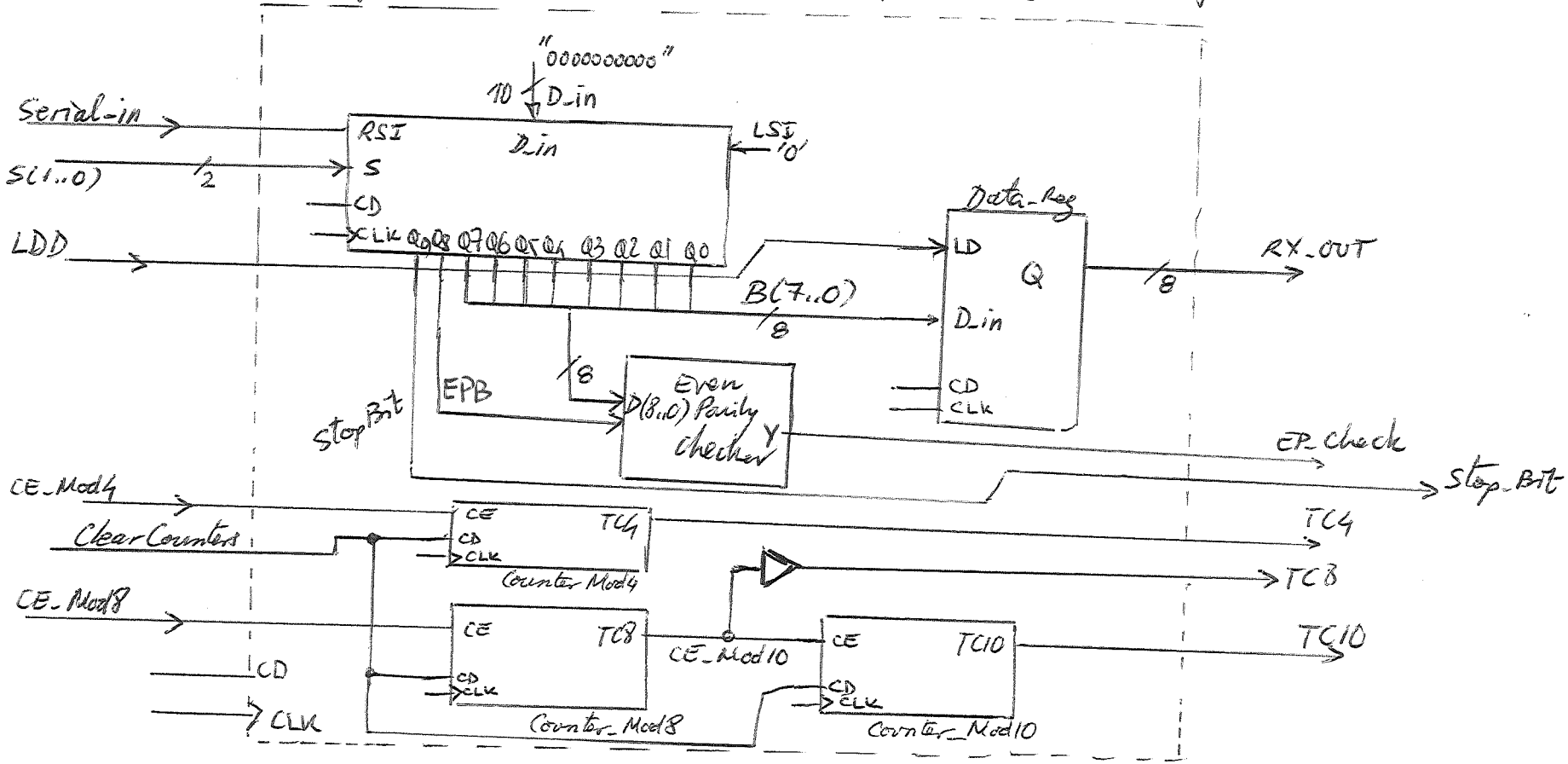
- The receiver control unit will be waiting for the falling edge and a low level in the serial_in
- a set of counters will be needed for
  - Counting a 4 cycle delay to be able to get a sample of the start bit
  - Counting a 8 cycle delay to be able to sample at the middle of every incoming bit
  - Counting up to 10 bits



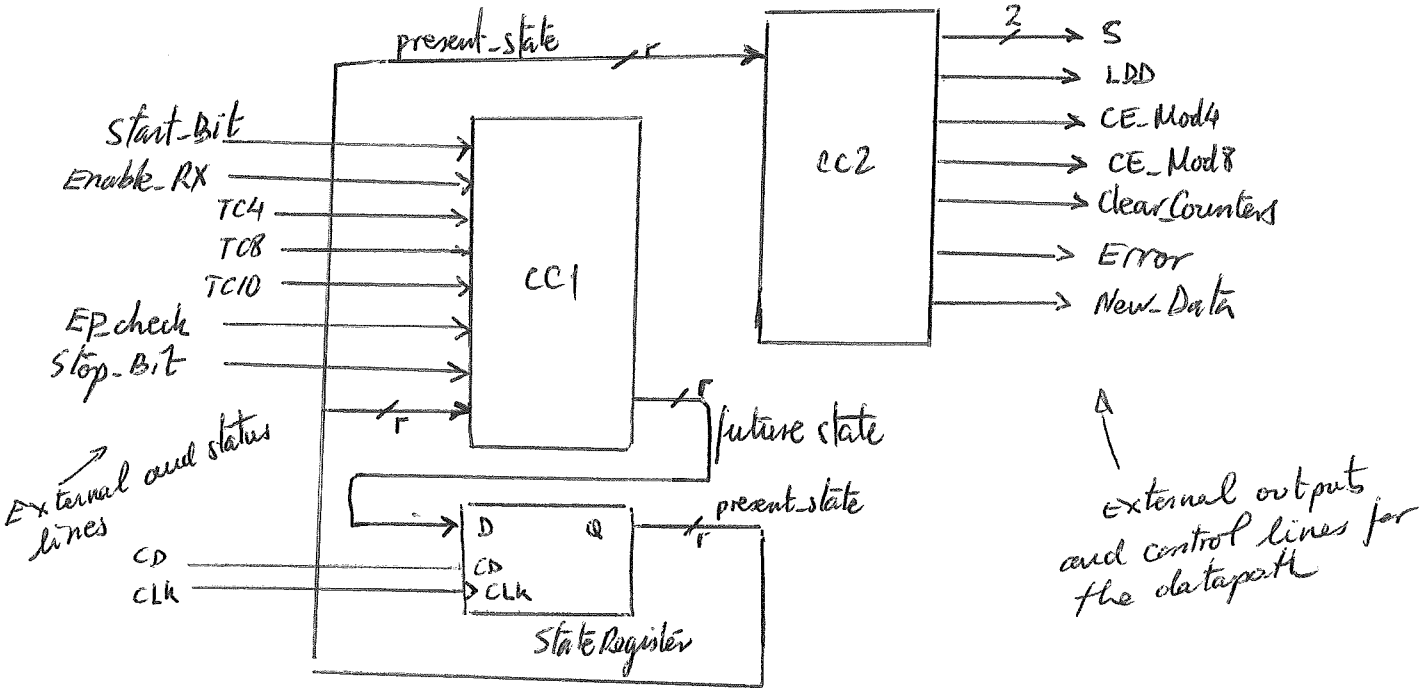
(2)



TC10 will be high after 10 pulses, and the sampling cycle will finish



Receiver control unit



This is only a possible proposal which may include some changes